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VOICE OF THE ENGINEER

MAY 24
Issue 11/2007
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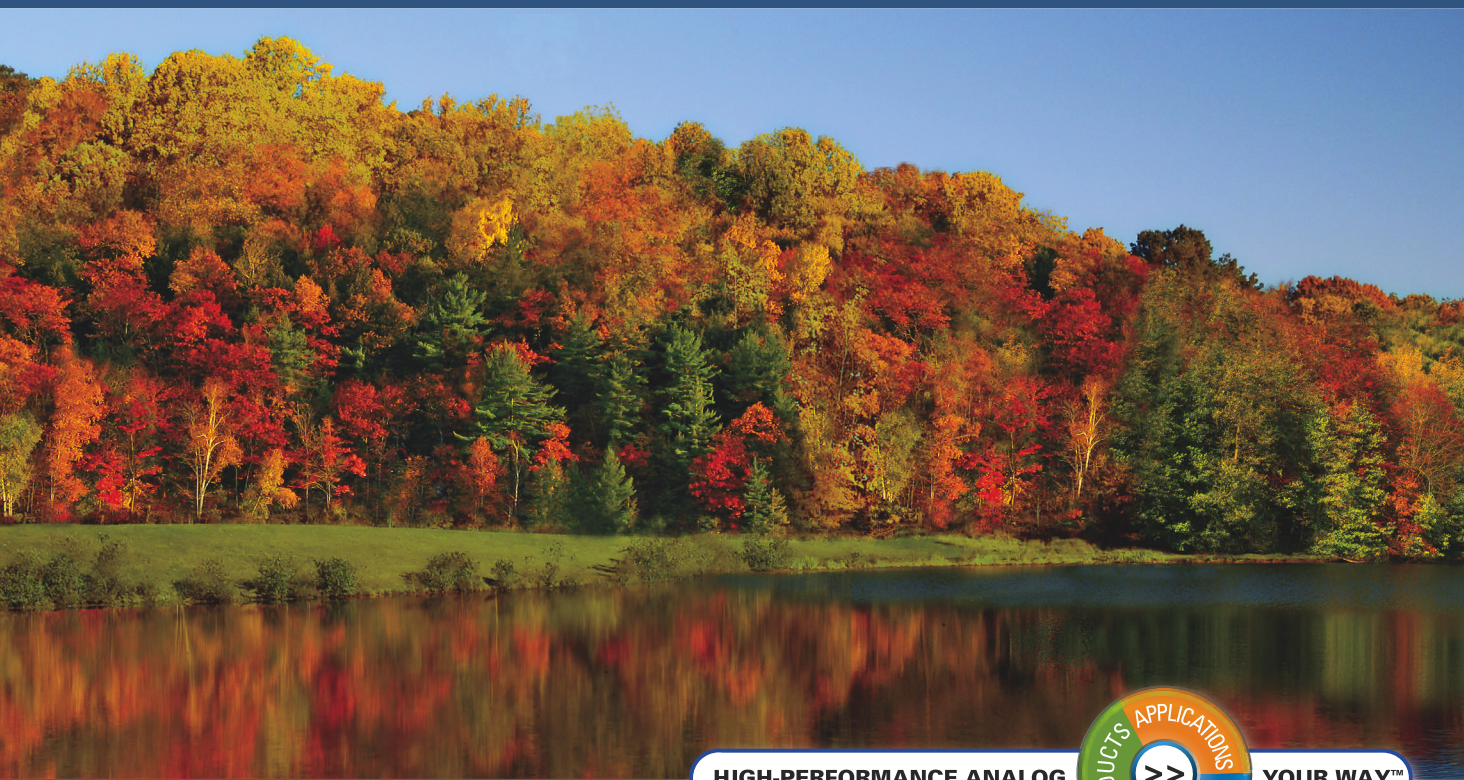
TAKING A BITE OUT OF POWER: TECHNIQUES FOR LOW-POWER-ASIC DESIGN

Page 46

Digital Power for a Changing World

Adaptable, High-Density, Multi-functional POL Controller



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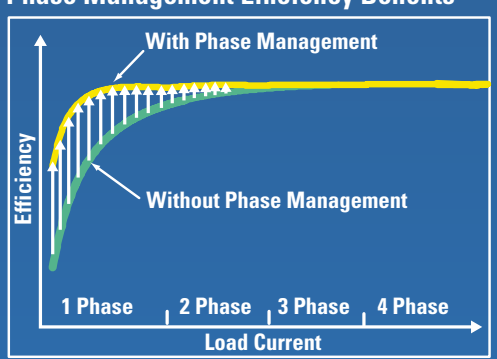
PRODUCTS APPLICATIONS SUPPORT

The new UCD9240 Fusion Digital Power™ point-of-load (POL) controller from Texas Instruments gives designers faster time to market without sacrificing features or performance. This flexible and adaptable multi-rail controller provides high power density, dynamic power supply, load-optimized phase management and configurable sequencing.

Phase Management Efficiency Benefits



High-Performance Analog >>Your Way

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- Data Acquisition Systems
- Modulators/Filters

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- Battery Management
- Charge Pumps
- DC/DC Switching Controllers
- DC/DC Switching Converters
- Digital Power
- Display Drivers
- Hot Swap
- LED Drivers
- Linear Regulators
- MOSFET Drivers
- Plug-In Modules
- Power Factor Correction
- Power Supply Control

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- Circuit Protection
- Digital Isolators
- Display Interface
- LVDS/MLVDS
- PCIe/PCI
- RS-485, 232 & 222
- SCSI
- Serializers
- Deserializers
- Transceivers
- UARTs
- USB

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- Analog ASSPs
- Analog MUXs
- Clocks & Timers
- Comparators
- Current Shunt Monitors
- Digital Up Converters
- Digital Down Converters
- Fan Controllers
- ISM Band
- References
- Switches
- Temp Sensors
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HIGH-PERFORMANCE ANALOG PRODUCTS APPLICATIONS SUPPORT >> YOUR WAY

Texas Instruments offers a comprehensive high-performance analog portfolio from amplifiers and data converters to power management and interface. Whether you need faster speed, higher precision, lower power or smaller size, TI has analog ICs to differentiate your design. That's High-Performance Analog >> Your Way.

OPA211	**Low-noise, low-power, 36V bipolar op amp** (1nV/√Hz; 3.5mA) in small MSOP-8 package
OPA333	**Lowest power, zero-drift op amp:** 2µA offset, 17µA current, SC70 and SOT23 packages
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ADS5546	**Fastest 14-bit ADC (190MSPS)** 73.2 SNR at 70MHz IF; 84dBc SFDR at 70MHz IF; 1.1W power
ISO721	**High-speed digital isolator:** 4000V (peak) isolation; signaling rate of 0-150Mbps; high electromagnetic immunity; low input current requirement; failsafe output
TAS5261	**PurePath Digital™ amplifier** capable of driving more than 300W
TPS63000	**96% efficient buck-boost converter** with up to 28% greater run-time; 3 x 3 mm² QFN package
TPS40140	**Stackable, scalable, flexible PWM buck controller** generates 10A to 320A of output current and enables maximum efficiency up to 16 phases

www.ti.com/analog

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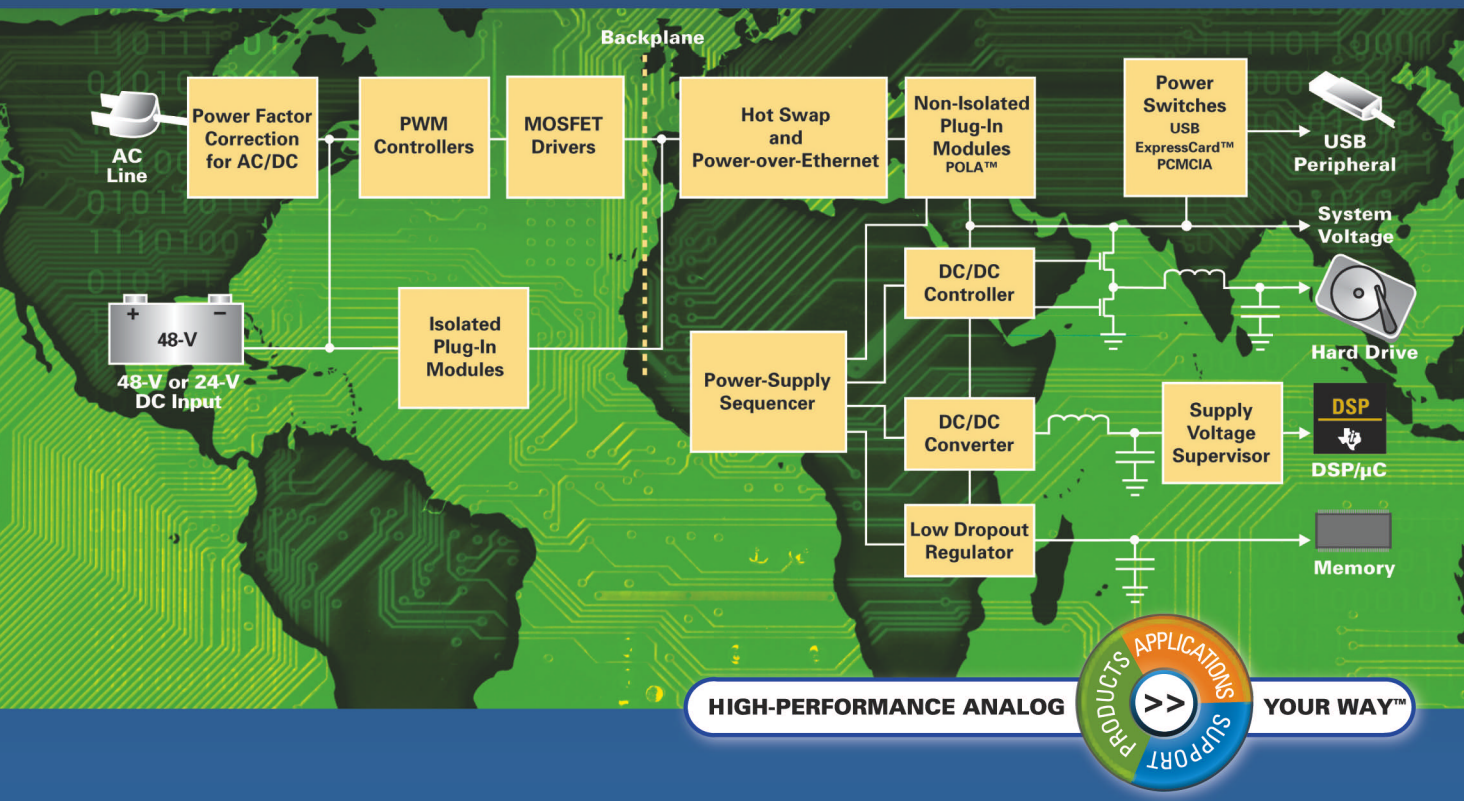
Power From AC Line to POL

High-Performance Analog >> Your Way™



TI's broad portfolio of line power solutions includes AC/DC and DC/DC conversion, digital power, hot swap, MOSFET drivers, PoE controllers, plug-in modules and power switches. With design software, reference designs, on-line training, local support and more, TI has the tools you need to meet your design challenges. That's High-Performance Analog>>Your Way.

UCC28600	8-pin offline quasi-resonant converter offers exceptional efficiency at high and standby power levels
UCC27200	120-V high-side, low-side MOSFET 3-A driver improves efficiency of half-bridge topologies
TPS40140	1 stackable 2-channel multiphase or 2-channel independent output DC/DC controller
TPS5430	Easy-to-use 5.5-V to 36-V input, 500-kHz, 3-A SWIFT™ DC/DC converter
TPS2410/1/ TPS2412/3	ORing-diode FET controllers reduce power loss and protect server and telecom power systems from transient events
PTH08T230W	6-A, 4.5-V to 14-V input, non-isolated, wide output-adjustable power module with TurboTrans™ Technology
PTQB425080	200-W, 48-V input, 8-V output, isolated DC/DC bus converter
DCH0105	Miniature 1-W, 3-kVDC isolated DC/DC converter

NEW Power Management Selection Guide, design software and reference designs >>

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Portable Power Management

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TI delivers high-performance and integrated power management solutions to fit battery power design challenges for a variety of applications, including cell phones, digital cameras, notebook computers and more. TI's applications knowledge and unique manufacturing capabilities, combined with local technical support, allow us to deliver innovative power management products for the most demanding portable power designs. That's High-Performance Analog >> Your Way.

TPS63000	**96% efficient, buck/boost DC/DC converter:** 1.2-A, in 3 x 3 mm^2 QFN
TPS799xx	**Low-noise, low dropout regulator:** 200-mA, 40-µA I_Q, high PSRR, in WCSP
TPS62110	**1.5-A step-down DC/DC converter:** synchronous, 17-V_{IN}, up to 95% efficiency
TPS62350	**800-mA step-down converter with I²C:** 3-MHz, 2.7-V to 6-V_{IN}, in WCSP
TPS61081	**High-voltage boost converter:** 27-V_{OUT}, integrated 1.3-A switch
bq24060	**Linear 1-cell, Li-Ion battery charger:** thermal regulation, 6.5-V OVP, temp sense
bq20z90	**Li-Ion battery gas gauge:** 99% accuracy, Impedance Track™ Technology, SBS 1.1-compliant
TPS65050	**6-channel PMU:** 2 DC/DCs and 4 LDOs, 4 x 4 mm^2 QFN, up to 95% efficiency
TPS65023	**6-channel PMU with I²C:** 3 DC/DCs and 3 LDOs, DVS, in 5 x 5 mm^2 QFN

Get samples, evaluation modules and access the online Power Management search tool at >>
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Industry's First 6V to 100V Current-Mode Buck Controller

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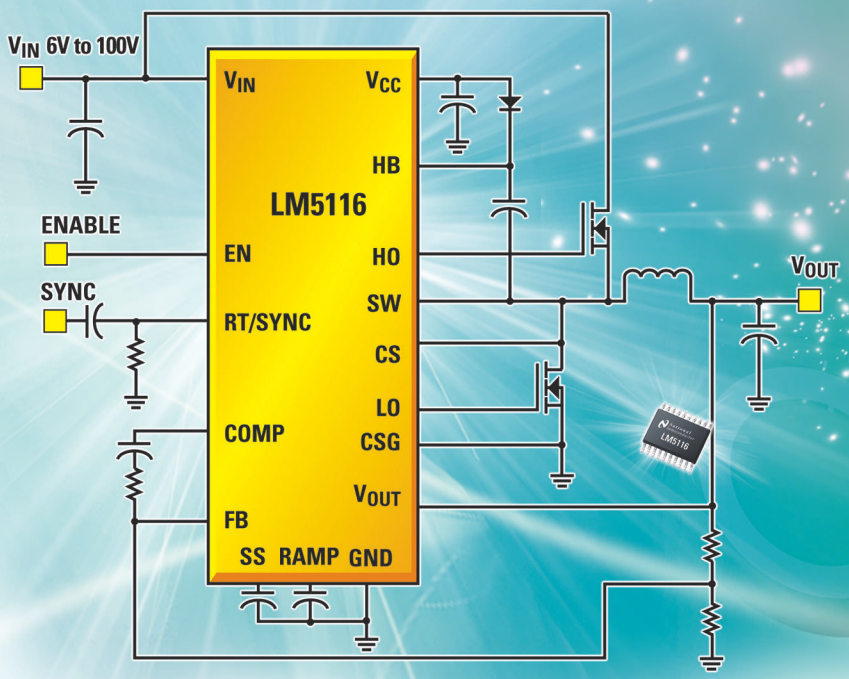
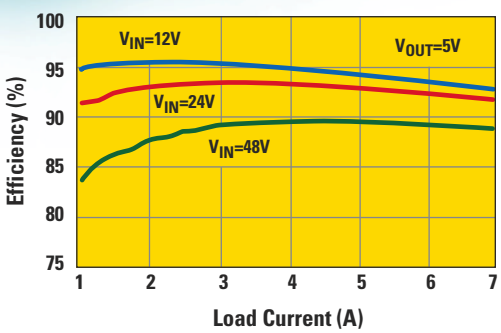
LM5116 Synchronous Controller Features Emulated Current Mode (ECM) Control for High Step-Down Ratio



LM5116 Features

- Ultra-wide input range: 6V to 100V
- Programmable output from 1.215V to 80V
- Less than 10 µA I_q in sleep mode
- Frequency adjustable to 1 MHz with sync capability
- Programmable soft-start
- Drives standard or logic-level MOSFETs
- RDS($_{ON}$) or resistor current sensing
- Controlled start-up into pre-biased load
- Available in thermally enhanced TSSOP-20 packaging

Typical Circuit Efficiency



Ideal for use in telecommunications, automotive, and industrial control applications

For FREE samples, datasheets, and more information on the LM5116, contact us today at: power.national.com

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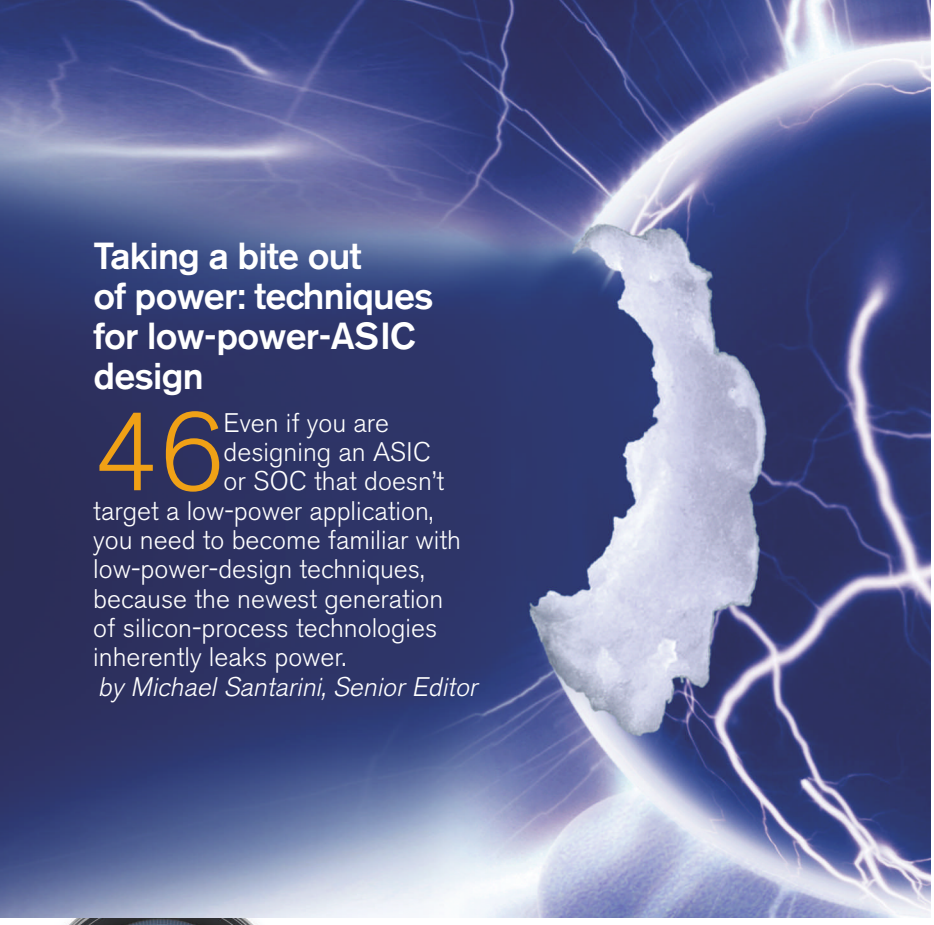

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Taking a bite out of power: techniques for low-power-ASIC design

Compact imaging systems face partitioning issues

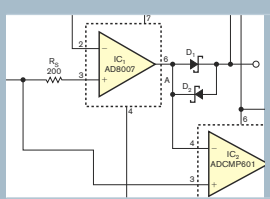
Estimating the ZigBee transmission-range ISM band

Designing medical devices for isolation and safety

Reducing power consumption in battery-powered applications

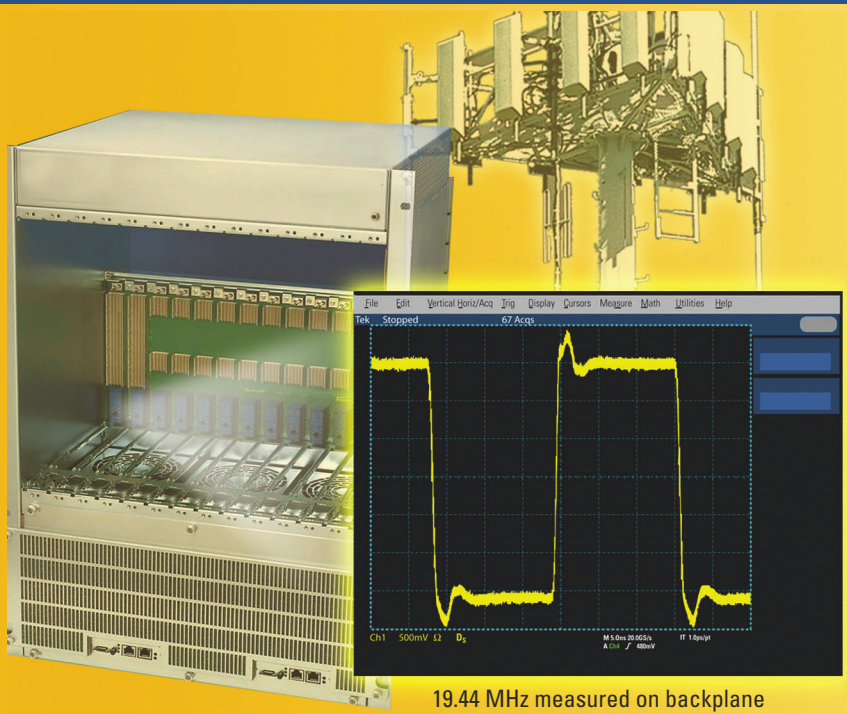
Small, high-performance ICs require wafer-level-RF measurements

DESIGNIDEAS



M-LVDS – The Bus Standard

Signal Integrity for Backplanes and Cables



19.44 MHz measured on backplane

Applications

- AdvancedTCA (ACTA) and MicroTCA
- Clock, data, sync and control
- Cellular base stations
- Central-office switches
- Test and measurement

Features

- Meets M-LVDS (TIA/EIA-899)
- 11.3mA driver output current
- 50mV receiver thresholds
- Contention provisions:
  - Driver short-circuit limited to 43mA
  - Devices limit bus voltage from 0 to 2.4V
  - Drivers tested with 32 contending nodes
- Failsafe support

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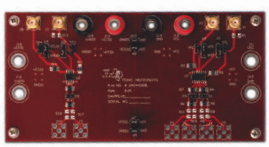
Texas Instruments provides a broad range of innovative Multipoint LVDS (M-LVDS) devices that deliver the speed, power and robustness required for backplane and multipoint bus applications. With contention features for data and control signals, single- and eight-channel transceivers, a quad driver, single-channel receivers, and clock buffer devices for 1:8 and dual 1:4 fan-outs, TI's M-LVDS products are ideal for distributing clock and synchronization signals.

Device	Signaling Rate (Mbps)	No. of Tx / Rx	Input	Output	ESD HBM (kV)	Function
SN65MLVD047A	200	4/0	LVTTL	M-LVDS	9	Quad Driver
SN65MLVD080	250	8/8	LVTTL, M-LVDS	M-LVDS, LVTTL	8	Octal Half-Duplex Transceiver
SN65MLVD128	250	8/1	LVTTL	M-LVDS	9	Repeater
SN65MLVD201	200	1/1	LVTTL, M-LVDS	M-LVDS, LVTTL	8	Half-Duplex M-LVDS Transceiver
SN65MLVD207	200	1/1	LVTTL, M-LVDS	M-LVDS, LVTTL	8	Full-Duplex M-LVDS Transceiver
SN65MLVD2	250	0/1	M-LVDS	LVTTL	8	Single Channel M-LVDS Receiver
SN65MLVD3	250	0/1	M-LVDS	LVTTL	8	Single Channel M-LVDS Type-2 Receiver

New products listed in red



For evaluation modules, data sheets and samples visit >> **www.ti.com/mlvds**

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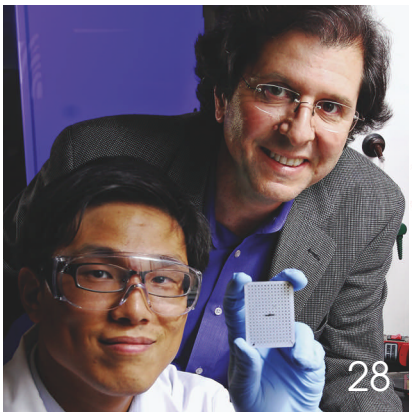

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DEPARTMENTS & COLUMNS

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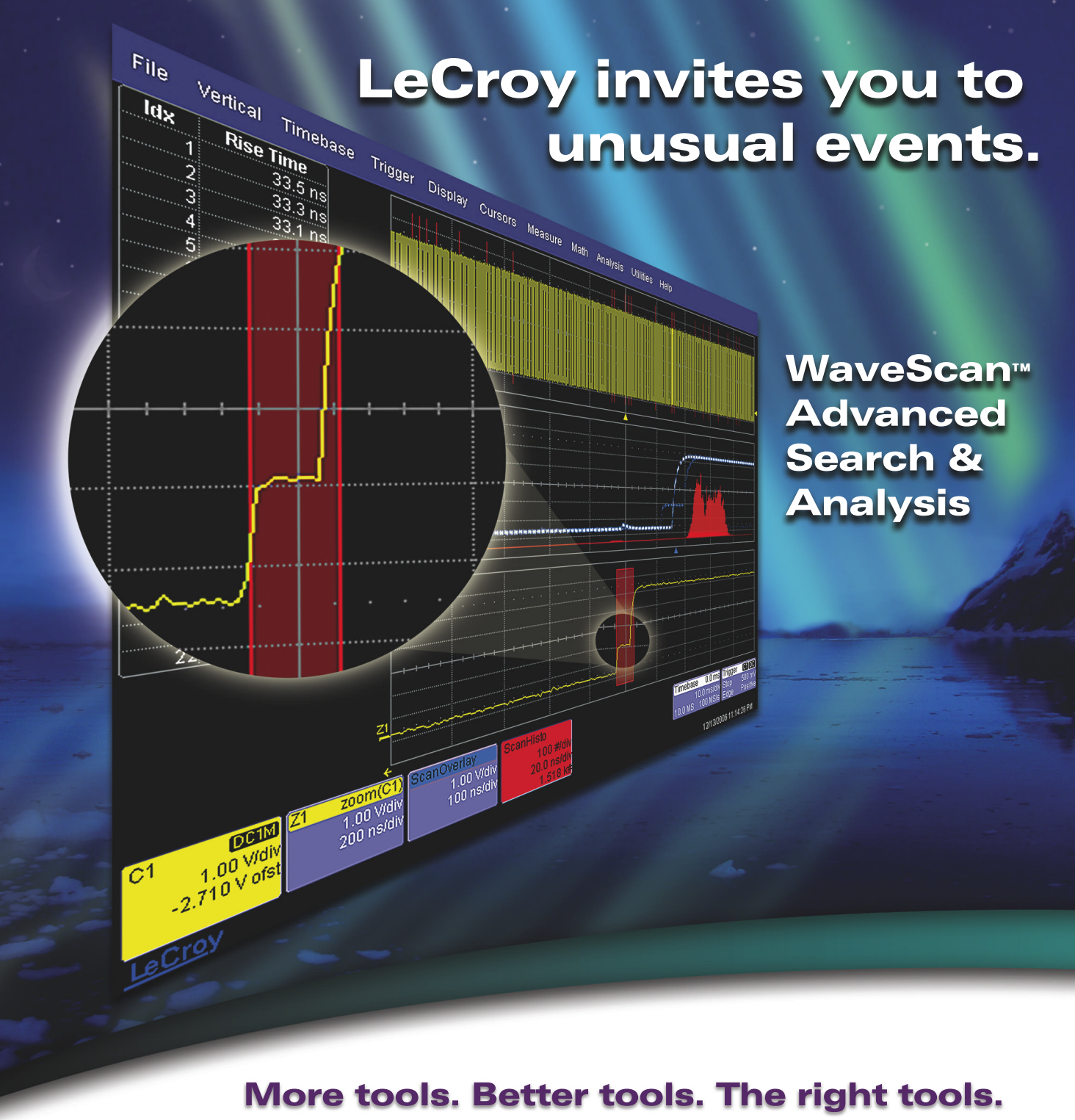

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EDN Magazine has included LeCroy's WaveRunner® Xi and WaveSurfer® Xs with WaveScan in it's 'Hot 100 Products' list. WaveScan is also an EDN 2007 Innovation Award Finalist.

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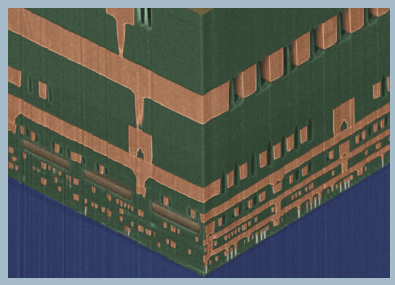

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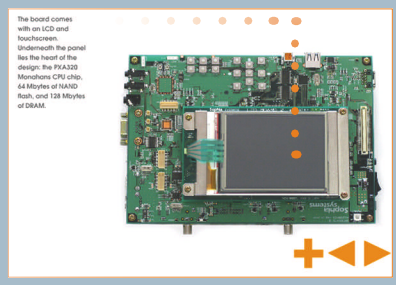

PRYING EYES COMES ALIVE

EDN's Prying Eyes articles, in which we tear into a product to reveal the engineering behind it, have proved popular. So we're now giving you the chance to explore some Prying Eyes projects in a multimedia Flash presentation. Check out:

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Exploring the foundation under smartphones
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A HEX (CODE) UPON US

In "Find hex-code values for microcontroller's ADC voltages" (April 12, 2007, www.edn.com/article/CA6430339), we flubbed a key formula. The typo made the Design Idea seem less impressive than it actually is and prompted some colorful reader comments. We have now corrected the online version, and the author has provided a look-up table, a handy Excel spreadsheet that allows you to interact with the formula, and some comments of his own.

SOME SHORTCUTS

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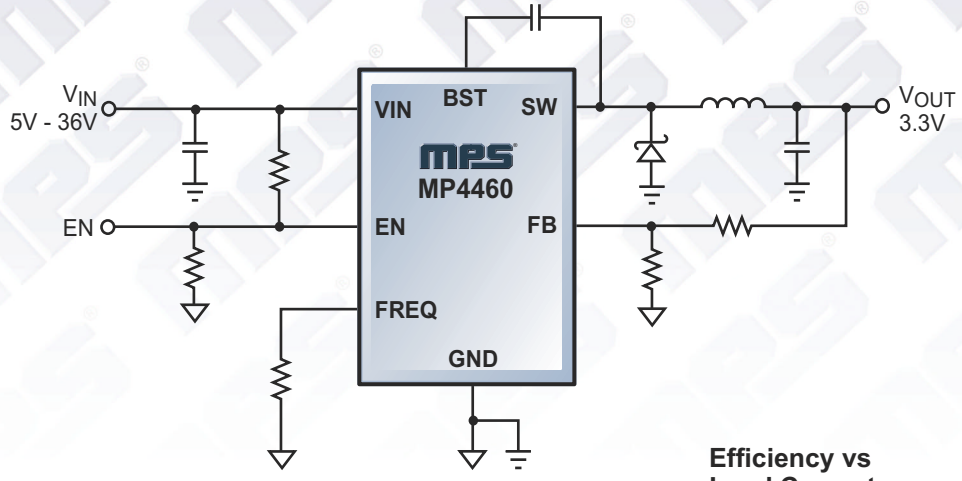
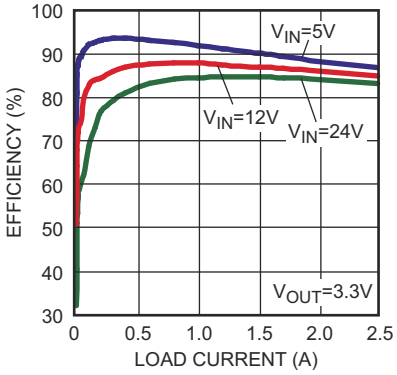
40V, 2.5A
Non-Synchronous Buck Regulator

Ultra Compact, Simplified Design Solutions



- *Adjustable Frequency Up to 4MHz*
- *Input Range 4.5V - 40V (Max)*
- *150mΩ Integrated Switch*
- *Compact QFN10 (3mm x 3mm) Package*
- *Only 10 External Components!*

Efficiency vs Load Current



Featured (High-Voltage) Non-Synchronous Bucks

Part	Frequency	V_{IN} (V)	V_{OUT} (V)	I_{OUT} (A)	Package
MP4459	4MHz (Adj.)	4.5 - 40 (Max)	0.8 - 36	1.5	TQFN10 (3mm x 3mm)
MP4460	4MHz (Adj.)	4.5 - 40 (Max)	0.8 - 36	2.5	QFN10 (3mm x 3mm)
MP2467	500KHz (Fixed)	6 - 40 (Max)	0.8 - 30	2.5	SOIC8E
MP4461	4MHz (Adj.)	4.5 - 40 (Max)	0.8 - 36	3.5	QFN10 (3mm x 3mm)

DC to DC Converters CCFL / LED Drivers Class D Audio Amplifiers Linear ICs

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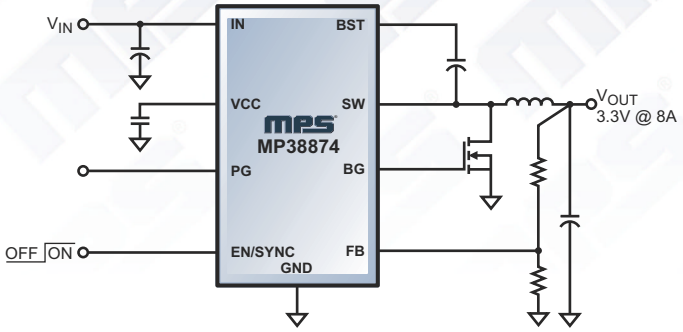
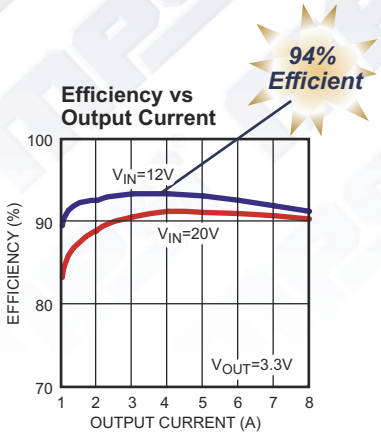
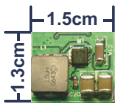
Synchronous Buck Regulator

45mΩ Internal Power MOSFET Switch

Only 8 External Components!







Actual Double Sided Footprint Solution Size

- *Up to 8A for Today's High Performance Digital Core*
- *Stable with Low ESR Output Ceramic Capacitors*
- *Internally Compensated*
- *Integrated Soft Start*

Featured (High-Current) Synchronous Bucks					
Part	**Frequency**	**V_{IN} (V)**	**V_{OUT} (V)**	**I_{OUT} (A)**	**Package**
MP38872	600KHz	4.5 - 21	0.8 - 15	6	QFN 14 (3mm x 4mm)
MP38891	400KHz	4.5 - 30	0.8 - 15	6	
MP38874	600KHz	4.5 - 21	0.8 - 15	8	

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BY MAURY WRIGHT, EDITORIAL DIRECTOR

Unique IP addresses will prove main IPv6 benefit

Starting in late 1999, I was editor of *CommVerge*, a short-lived sister publication to *EDN* that focused on the convergence trend. We launched just as the Internet went mainstream and folded with the so-called dot-com bust. In the first issue, my article "Maxed out" described the critical need for a move from IPv4 (Internet Protocol Version 4) to IPv6 (Internet Protocol Version 6) as the foundation of the the burgeoning Internet (www.edn.com/article/CA41781). My primary thesis centered on the shortage of unique IP addresses that 32-bit IPv4 afforded. Now, a number of measures, such as NAT (network-address translation), seemingly have solved the address issues—or have they? Many good reasons still exist for devices to have globally unique IP addresses.

Acquaintances that use technology but aren't in the tech industry have been asking me about the concept of a new Internet to replace what we have. I think it's highly unlikely that we can develop an entirely new network and one day throw the switch to move from old to new, although I can see the clean-sheet-of-paper benefits when things such as security are concerned. I believe that it's more likely that we will continue to evolve the Internet and that a move to IPv6 almost a decade after I first thought it was a critical need would be a step in the right direction.

For a good update on the status of IPv6, you might check out a comprehensive package of stories that *eWeek* produced on the subject. The main story, "IPv6: Ready or not," and numerous sidebars describe the advantages of IPv6 and the obstacles to broad deployment (www.eweek.com/article2/0,1895,2126069,00.asp). The main *eWeek* article used the Katrina hurricane disaster to point out how IPv6 could have greatly improved quick deployment of a network after such a disaster. Quicker and simpler deployment would have accelerated recovery efforts. IPv6 would have simplified deployment because every IP-enabled device, including notebooks and even cell phones, could act as a server on the network, providing an immediate means to dynamically build a network.

It's highly unlikely that we can develop an entirely new network and one day throw the switch to move from old to new.

I'd argue that IPv6 is also great in the embedded-device market in which more machines, sensors, and other noncomputer devices are network-enabled. Indeed, I'd encourage all engineers to design for IPv6 support even if they don't think that support is currently necessary. I'm hoping that IPv6 has simply been another victim of Leibson's Law (www.edn.com/blog/980000298/post/750007875.html). Steve Leibson, a Tensilica executive, *EDN* contributor and blogger, and former *EDN* editor in chief, observed that it takes any good idea a decade to matriculate and succeed. IPv6 was stable and ready for prime time around 1999. We should see a broad migration to IPv6 in the next few years.

Alas, I always expect technology change to happen more rapidly. Clearly, I was early in calling for IPv6 adoption at the beginning of 2000. At the time, it seemed necessary. I remember companies such as 3Com and Cisco having hordes of IP-address space and giving every employee a unique IP address, although, in their labs, they were working on NAT and similar technologies. Who knew that every wired home would have a NAT-enabled router and that broadband providers would dynamically assign IP addresses? I guess I can take solace in not being the only person alarmed by the disappearing address space.

I could have also used a dose of Leibson's Law before I wrote the editorial for that first issue of *CommVerge*. In "POTS: R.I.P.," I predicted the demise of analog telephones and a massive switch to VOIP (voice over IP) within a year or two (www.edn.com/article/CA41788). Well, I still have a POTS (plain-old-telephone-system) phone today. But here we are, more than seven years later, and VOIP is rapidly usurping POTS, and, by the time the clock strikes a decade, POTS will likely be gone. EDN

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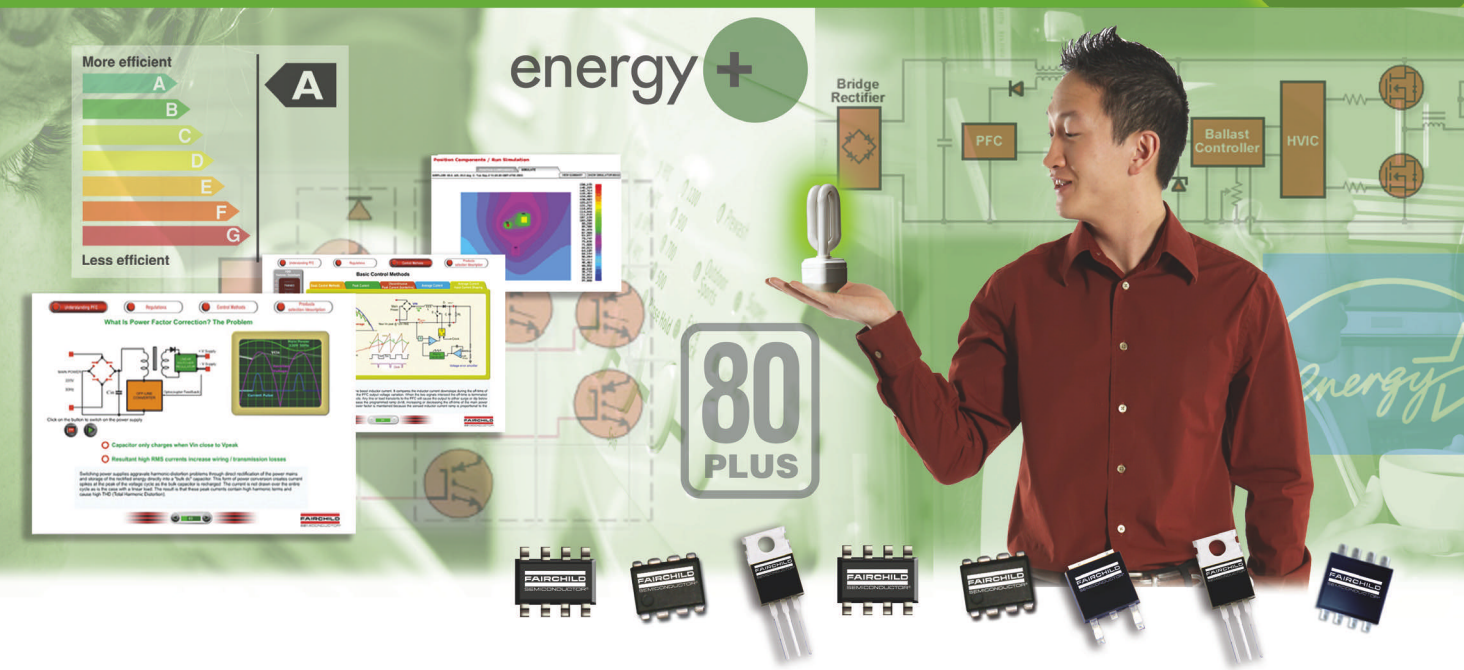

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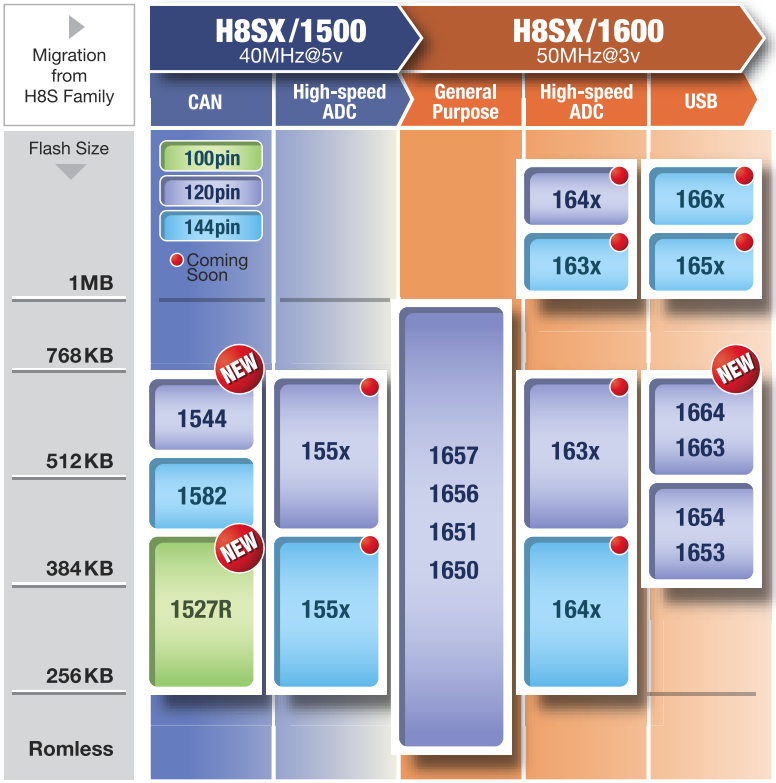

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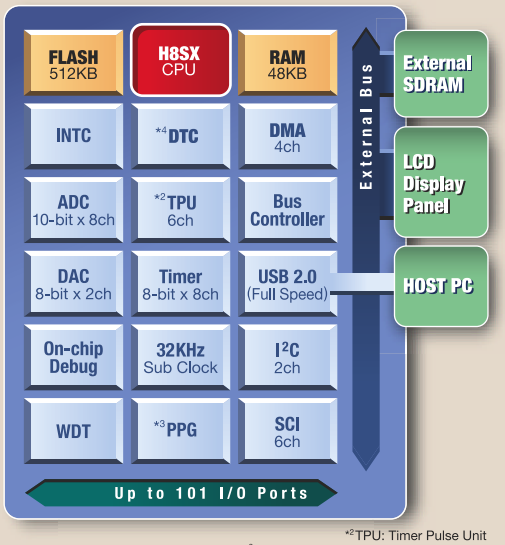

*2TPU: Timer Pulse Unit
*3PPG: Programmable Pattern Generator
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Minimizing FET Losses for a High-Input Rail Buck Converter

Application Note AN-1628

William Stokes, Applications Engineer

Engineers often face the challenge of choosing the input voltage rail that works best for the DC-DC converter at the Point-of-Load (POL). High voltage rails, above 12V, usually demand intermediate regulation stages that reduce overall efficiency and add to cost. However, the new generation of regulator and controller ICs afford POL regulation from these high input rails directly. Typically the buck regulator is employed as the POL workhorse but its efficiency is highly dependent on the optimization of the High-Side (HS) and Low-Side (LS) MOSFET (FET) combinations. At lower input voltages it is often possible to use the same HS and LS FETs, yet for higher input voltages the selection criteria for these FETs are different, and will be the subject of this application note.

Buck Converter Loss Mechanisms

The schematic in ***Figure 1*** shows the basic architecture for a DC-DC buck (or step-down) voltage regulator circuit that employs the LM5116 as the Pulse Width Modulator (PWM) switch controller. The critical current path is from V_{IN} through the HS FET to the output via the inductor; and alternately, from ground through R_S and the LS FET to the output. Power losses due to the FETs along this path tend to dominate all other losses.

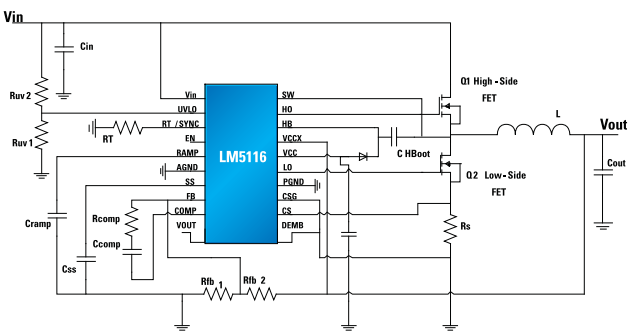

Figure 1. Synchronous Buck Regulator Schematic

Losses occurring in the FETs are a combination of conduction losses in the channel of the FET and switching losses during the turn-on and turn-off transitions. Conductive losses are proportional to the RMS current through each FET, and ignoring the ripple current in the output inductor, are often approximated (for the HS and LS respectively) by the following:

$$P_{QHS} = I_{OUT}^2 \cdot R_{DHS} \cdot D \text{ and}$$
$$P_{QLS} = I_{OUT}^2 \cdot R_{DLS} \cdot (1-D) \quad \text{(Eq. 1)}$$

In these equations I_{OUT} is the output current, R_{DHS} and R_{DLS} are respectively the on-resistances of the HS and LS FETs, D is the duty cycle of the HS FET and $(1-D)$ is the duty cycle of the LS FET.

The duty cycle, D, is given by $D = \frac{V_{IN}}{V_{OUT}}$ **(Eq. 2)**

The switching behaviors of the HS and LS FETs in the buck regulator differ from each other and this difference can be understood with the aid of ***Figure 2.***

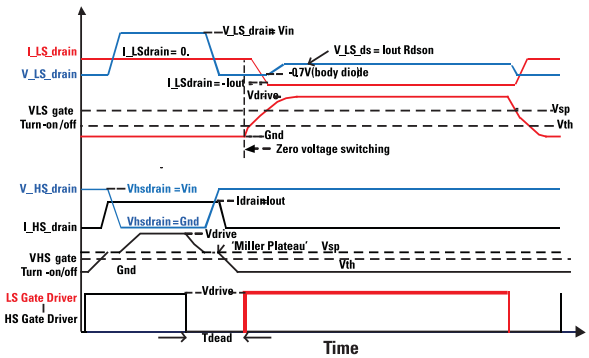

Figure 2. Basic Switching Characteristics (not to scale) for HS and LS FET Operating in a DC-DC Converter Application

The LS FET exhibits zero-voltage switching. First of all, the gate voltage, V_{LSgate}, turns the FET on while the FET's body diode is conducting. Then, when the gate turns the FET off, the load current will continue to flow in the same direction but now through the body diodes, such that the drain voltage stays near zero. Thus the attendant switching losses are negligible in both cases.

The main switching loss caused by the LS FET occur in the gate driver due to the charging and discharging of its gate capacitance. At higher frequencies in high power systems this can impose an upper limit on the number of LS FETs that can be used in parallel to reduce the on-resistance. The increase in gate drive power required as more FETs are used in parallel can exceed the reduction in conduction losses.

Switching losses are significant in the HS FET because its drain-source voltage is equal to V_{IN} and its drain current is approximately equal to I_{OUT} at both turn on and

turn off, leading to large overlap losses. The switching losses are approximated by

$$Psw_{Q1} = \frac{1}{2} \cdot V_{in} \cdot I_{out} \cdot f_{sw} \cdot (tsw_{HS\_rise} + tsw_{HS\_fall}) + Q_{gs} \cdot V_{GH} \cdot f_{sw} + \frac{1}{2} \cdot C_{oss} \cdot V_{in}^2 \cdot f_{sw}$$

(Eq. 3)

where f_{SW} is the switching frequency; tsw_{HS_rise} is the time it takes the gate voltage to rise from its threshold value to the end of the plateau interval; tsw_{HS_fall} is the time it takes the gate voltage to fall from the beginning of the plateau interval to the threshold value; Q_{gs} is the total gate charge of the FET; C_{oss} is the FET's drain-source capacitance; and V_{GH} is its gate drive voltage. The determination of the fall and rise times is beyond the scope of this article, but the relevant equations can be found in the web-published application notes of various MOSFET vendors.

The first term on the right hand side in ***Eq. 3*** is the power lost in the FET due to the simultaneous high drain current and drain-source voltage at turn on and off already mentioned. The second term is the power required by the FET's gate, (which is dissipated in the gate driver). The third term is the power dissipated in charging the parallel combination of the LS and HS FETs' output capacitance.

Another switching loss that occurs in the HS FET is due to the reverse recovery of the LS FET's body diode. This loss can be virtually eliminated at low currents (<5A) by paralleling a schottky diode with the LS FET.

Design Lessons

The following generalizations are based on the above equations and should give further insight into FET selection:

1) Switching losses increase for larger gate and drain capacitance and these capacitance are inversely proportional to the on-resistance. FETs with the lowest on-resistance inevitably have the higher capacitance hindering HS switching speed.
2) Reducing the switching clock frequency reduces switching losses; that is, at lower frequencies the losses during on/off transitions become a diminishing proportion of the total on-time of the FET causing conduction losses to increasingly dominate.
3) For higher input voltages relative to the output voltage the duty cycle of the HS FET decreases causing the switching losses to increasingly dominate.
4) In order to further reduce conduction losses, multiple, parallel, LS FETs are often employed. The number of parallel FETs is determined ultimately by cost, the gate driver's ability to drive them, and the point of diminishing returns.

The engineer should be aware that in most POL applications, especially for input voltages higher than 12V, the switching losses will likely dominate all other losses. ***Equation 3*** shows that under these circumstances the lowest overall losses in the HS FET are not necessarily achieved by using a device with the lowest on-resistance. The FET must be selected to minimize the sum of all the losses. The FET's on-resistance must be optimized at a higher value to achieve reduced capacitance and so reduce the switching losses. The major MOSFET vendors now provide "reduced charge, fast switching " MOSFETs which are optimized in this way for high-side buck applications.

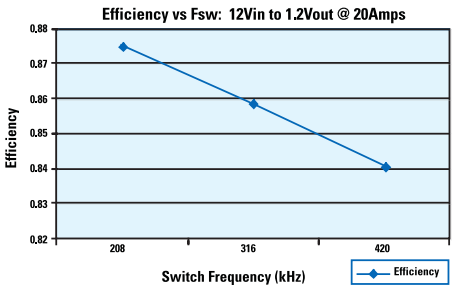

Figure 3. DC-DC Converter Measured Data Showing the Efficiency as a Function of the Switching Frequency

If optimizing the FETs does not enable high enough efficiency in a system, the switching frequency can be reduced to decrease the switching losses and improve the efficiency. This, however, can result in a physically larger system. ***Figure 3*** is an example of measured data from a generic evaluation board. The efficiency of this board was measured at various switching frequencies without changing any components on it except for the frequency-setting resistor. Though the conduction losses increased as the switching frequency was reduced (due to increased ripple currents), the overall efficiency went up because the switching losses in the HS FET decreased. The graph shows that changing the switching frequency has a dramatic effect on the switching losses.

The foregoing discussions have made clear that to achieve maximum efficiency in a high input voltage buck converter, the high side MOSFET must be carefully selected to minimize the sum of the switching and conduction losses. ■

The author wishes to acknowledge Haachitaba Mweene for his help with writing this article.

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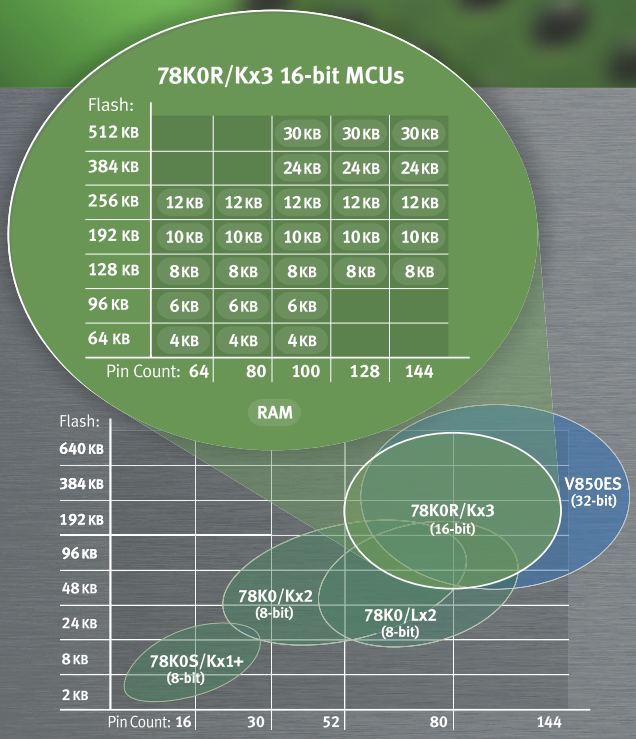

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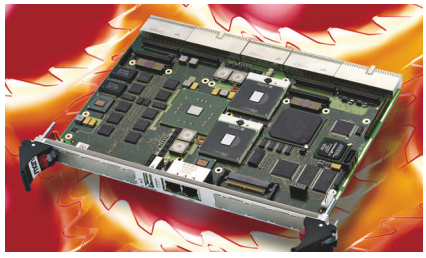
Blade computer sports four cores

Aiming to boost the performance of applications in the telecommunications, medical-engineering, and transportation industries, MEN Micro recently released a new 6U, CompactPCI single-board computer featuring either one or two Intel Xeon dual-core processors operating at 1.66 GHz. You can use the hot-swappable D7 server blade as a peripheral-slot board; a 64-bit, 66-MHz PCI system board; or a 64-bit, 133-MHz PCI-X (PCI Extended) system board. The D7 allows multiple memory variants, including error-correcting DRAM, nonvolatile FRAM (ferroelectric random-access memory), SRAM, and NAND flash. The built-in PCI Express link drives the two Gigabit Ethernet interfaces on the front panel and one or two XMC (switched-mezzanine-card) modules. The D7 also supports 12-Gbps Ethernet connections without performance losses.

In addition to a front-panel USB slot, the D7 includes two serial and two parallel ATA (Advanced Technology Attachment) interfaces for connection of mass-storage devices or CompactFlash. The D7 includes an FPGA for configuration of application-specific I/O functions, such as additional serial interfaces, graphics, fieldbus interfaces, and digital I/O. The price for the D7 is $5010, and delivery is within two weeks after receipt of order.



The new D7 CompactPCI single-board computer features dual-core processors, hot-swap functions, and a reconfigurable I/O section.

—by Warren Webb

▷**MEN Micro Inc**, www.menmicro.com.

FEEDBACK LOOP

"I had a hi-fi nut for a housemate a few years back. ... Unlike many, he didn't fall for the whole OFC (oxygen-free-copper) thing. Instead, he braided three or four pieces of multistrand, copper-mains-rated cable to produce flat, flexible cables. ... (It's) simple, safe, cheap, good listening ... can't get better than that!"

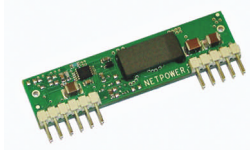
—Dean Perry, in *EDN*'s Feedback Loop, at www.edn.com/article/CA6418215. Add your comments.

Synchronizable POL converters beat the noise

Power subsystems that use a DPA (distributed-power architecture) usually have several independent power modules throughout the system, providing different voltages and currents and probably switching at different frequencies. These differing frequencies can cause significant noise problems for the system. The IBA (intermediate-bus architecture) is even more susceptible to module switching noise. It has more switching modules with higher switching currents resulting from the lower voltages of the architecture's nonisolated POL (point-of-load) converters. Add to this the fact that the power subsystems often mix power converters from different manufacturers, and a very noisy power environment can result.

To address these problems, the NAT1vvvXcc family of POL converters from NetPower includes a synchronization option to allow all POL converters in a system to operate at the same switching frequency and to eliminate beat frequencies. In addition, you can phase-shift the converters' clocks, allowing the converters to operate in an interleaved mode and further reduce switching-frequency noise. The synchronization also lets designers avoid critical frequencies that may interfere with the system's operation or modulate the switching frequency to eliminate or manage system EMC (electromagnetic-compatibility) problems. The input range for the modules is 8.5 to 18V, and the output range is 0.75 to 8V with a 12A ($9.30) or a 20A ($11.50) output current.**—by Margery Conner**

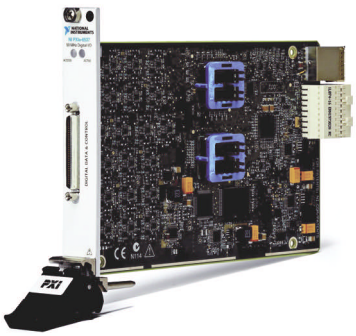
▷**NetPower**, www.netpowercorp.com.



The NAT1vvvXcc family of POL converters from NetPower includes a synchronization option to allow all POL converters in a system to operate at the same switching frequency and to eliminate beat frequencies.

100M-sample/sec, 14-bit digitizer and 25- and 50-MHz digital-I/O modules are first to support PXIe

National Instruments has announced what it calls the industry's first PXIe (PXI Express) high-speed instruments as well as the industry's first 18-slot PXIe chassis. The modular instruments include the 100-MHz, 100M-sample/sec, dual-channel PXIe-5122 digitizer and the 50- and 25-MHz, 32-channel PXIe-6537 and PXIe-6536 digital-I/O modules. The PXIe-1065's 18-slot chassis offers dedicated bandwidth of as much as 1 Gbyte/sec per slot and both PXI and PXIe slots. According to the company, the PXIe products target applications such as signal intelligence, spectral monitoring, semiconductor-chip characterization, and video test.



The PXIe-6537, which interfaces through a one-lane PCIe high-speed, bidirectional serial bus, accepts 32 channels of digital I/O with data rates as high as 50 MHz per channel.

"PXIe builds on commercial PCIe [PCI Express] technology to increase the number of applications the multivendor PXI standard serves," says Eric Starkloff, National Instruments' director of test-product marketing. "Adding a high-speed data-streaming capability to PXI maintains the compatibility among more than 1200 modules from more than 70 vendors that has made the standard a leading modular-instrumentation platform."

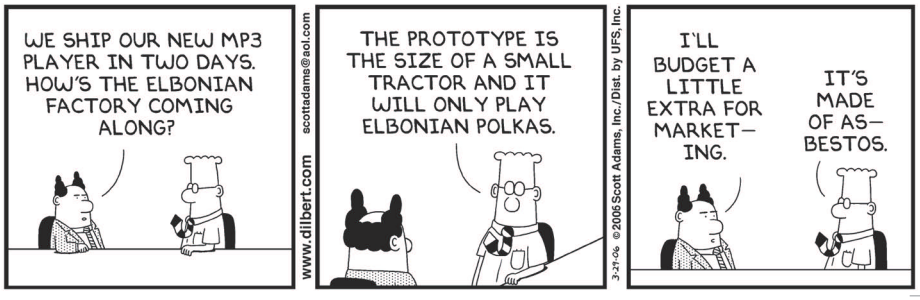
The new instruments add to the manufacturer's extensive list of PXI mixed-signal products, which include high-speed digitizers and oscilloscopes, high-speed digital-I/O modules, baseband and RF analyzers, and signal generators. The new instruments enable high-speed data recording and playback through the newest industry-standard bus, PCIe, which, on a bidirectional, four-lane link, delivers as much as 1 Gbyte/sec of streaming throughput. For example, with the four-lane-link-based PXIe-5122 digitizer, you can simultaneously capture analog signals on two channels with 14-bit resolution at 100M samples/sec and stream the signals across the PCIe bus to the PC's memory or hard disk at the digitizer's full rate of 400 Mbytes/sec. You can also use the X1-link-based PXIe-6536/37 digital-I/O modules to stream digital waveforms to and from the module at the full 200-Mbyte/sec data rate.

The PXIe-1065's 18-slot chassis complements the PXIe-1062's eight-slot chassis to address higher-channel-density PXIe-based systems. The new chassis includes a combination of PXI and PXIe hybrid slots to accept both current PXI modules and higher bandwidth PXIe modules. All of the PXIe products integrate with a variety of software, including the manufacturer's LabView graphical-development environment, LabView SignalExpress interactive-measurement software, and TestStand test-management software.

Prices for the PXIe-5122 digitizer, the PXIe-6536/37 digital-I/O modules, and PXIe-1065 chassis start at $5499, $1799, and $5499, respectively.**—by Dan Strassberg**

▷**National Instruments**, www.ni.com.

DILBERT By Scott Adams



AC/DC SUPPLY ACHIEVES 11.2W/IN.^{3}

05.24.07

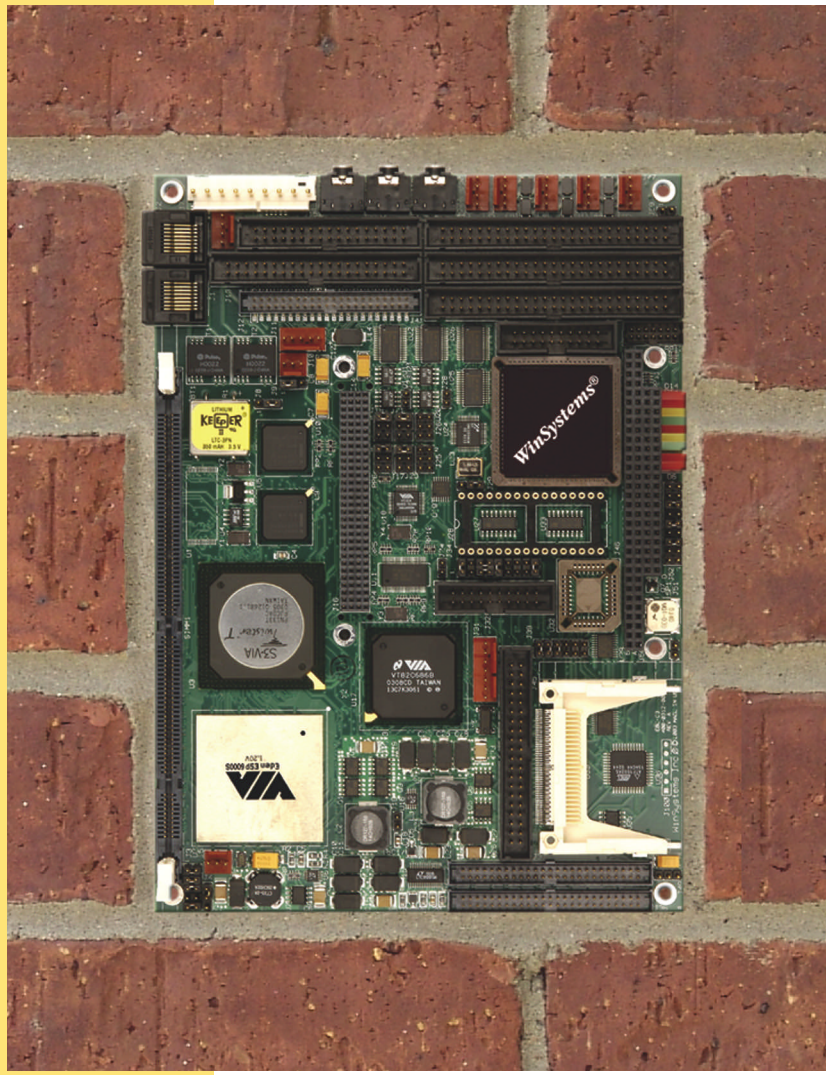
The MFA350 ac/dc-power supply from XP Power provides 350W in its 3.2×6.8×1.5-in. (81×173×38-mm), U-bracket package. The base product delivers 364W across the entire input range of 90 to 264V ac and is available in 12, 24, and 48V-dc-output versions. It includes a 12V, 1A fan supply and a 5V, 0.3A standby supply and signal set, including ac fail, dc OK, remote on/off, active current sharing, and remote sensing. The unit functions at full power from −10 to +50°C and at temperatures as high as 70°C with derating. The MFA350 is 89% efficient and requires 13-cfm airflow for full output power. Hot-swap models have ORing FET outputs, front-access IEC (International Electrotechnical Commission) inlets, and extraction handles. The supply fits a 1U×2U profile, allowing vertical or horizontal orientation in a standard telecom chassis. It costs $175 (OEM quantities).

–by Margery Conner

▶**XP Power, www.xppower.com.**

BUILT TO LAST

Fanless EBX 733MHz P3 with COM, dual ENET, USB and Video



- VIA 733MHz or 1GHz C3 CPU
- PC-compatible, supports Windows® XP, CE, Linux and x86 RTOS
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- Up 1GB bootable DOC®, 512KB SRAM, or 1MB EPROM
- Type I and II CompactFlash cards supported up to 8GB
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- Four USB ports
- Four serial COM ports
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- Two EIDE and one floppy disk controller
- AC97 Audio supported
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- +5 volt only operation
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The EBC-C3 embeds 9 different functions to provide a processor- and I/O-intensive solution. It operates over a -40° to +85°C temperature range without the need of a fan, making it ideal for embedded applications such as robotics, MIL/COTS, transportation, pipeline, and machine control.

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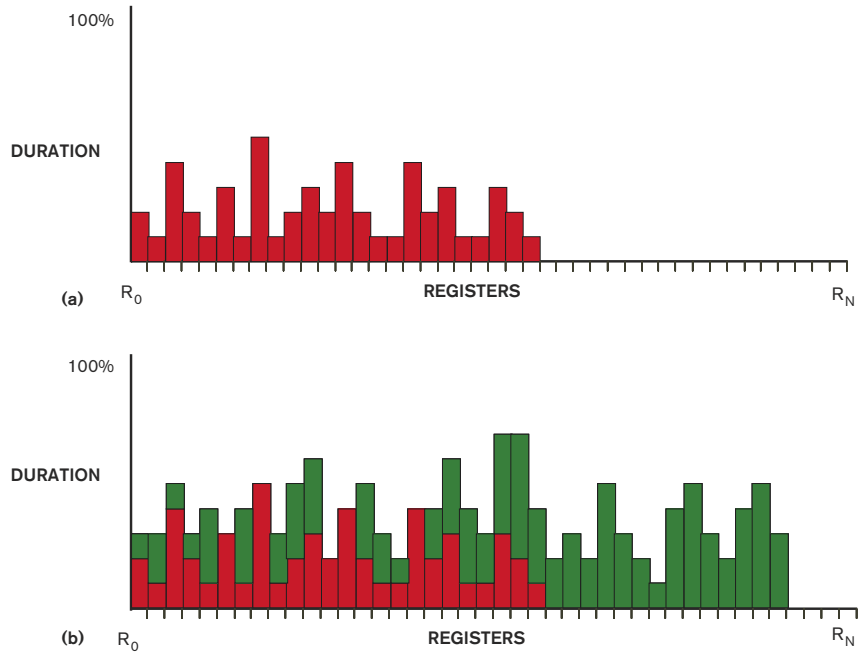
Linux

Calypto fields RTL-clock-gating tool



PowerPro CG finds more clock-gating opportunities and gates logic for longer times. In original designs, customers achieved efficiencies of 62.6 and 39.1% without PowerPro CG (a). Using the tool, the same customers achieved, respectively, 72.8 and 61.8% efficiency (b).

EDA start-up Calypto Inc has broadened its product portfolio beyond system-to-RTL (register-transfer-level) functional-verification tools with the introduction of an automated clock-gating tool for low-power-IC design. The PowerPro CG (clock-gating) tool complements the company's SLEC (sequential-logic-equivalence checker) CG, RTL, and other functional-analysis tools. PowerPro CG aims to help design engineers create low-power designs. The company claims that, using the tool, beta customers that were previously performing manual clock gating on their designs further reduced dynamic-power consumption by as much as 60%.

Tom Sandoval, chief executive officer of Calypto, says that one of the most popular ways that engineering teams reduce power consumption in IC designs is to gate clocks, but designers traditionally do most of the gating late in the design process at the gate level during layout; as a result, they must manually perform this task. With PowerPro CG, Calypto hopes to change that situation. The analysis-driven PowerPro CG allows designers to reduce dynamic power without impacting leakage power, area, or timing, according to Sandoval.

Designers will use the PowerPro CG with logic synthesis. They run the RTL versions of their designs in synthesizable Verilog or VHDL through synthesis to get a power figure. They then feed the raw RTL, an SDC (Synopsys Design Constraint) timing file, an SAIF (Switching Activity Interchange Format) file, and a Liberty Synopsys cell-library file to the PowerPro CG. The tool analyzes the RTL for clocks that designers can gate for further power savings. Users can select which clocks they want the tool to gate and select critical paths they don't want the tool to gate. The tool then analyzes the RTL and generates power-optimized RTL for the selected clocks. Users can then run SLEC CG to ensure that the power-optimized version of the RTL is functionally the same as the original RTL. Users can also then run the power-optimized RTL through logic synthesis.

The tool performs power optimization with no impact on timing, and, in most cases, the optimization reduces the overall die area the design requires. The tool takes advantage of the company's SLEC sequential-analysis engine, finding opportunities to reduce power that manual inspection misses. "If engineers spend enough time inspecting RTL and analyzing how it works sequentially, they can come up with these same transforms," says Sandoval. "But that task would be very difficult." He notes that, for efficient clock gating, a tool or an engineer must consider which logic to gate and for how long and then must consider the trade-off of gating versus area or performance.

"PowerPro optimization typically finds hidden opportunities for gating and opportunities to gate more obvious clocks for a longer period of time," says Sandoval. PowerPro CG runs under Linux and sells for $295,000 for an annual subscription.

—by Michael Santarini

▷**Calypto**, www.calypto.com.

FEEDBACK LOOP

"Engineers not only trade value for money, but also provide an opportunity for others to participate. As an engineer in an upstart, I have come to realize that there are dozens of people employed because I offered that trade, and there are hundreds of others that purchase my product and, through that, many more people are afforded a livelihood."

—Kevin Kilzer, in *EDN*'s Feedback Loop at www.edn.com/article/CA6409623.

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Atmel's AVR32 UC3 processor boasts low power

At last month's Embedded Systems Conference in San Jose, CA, Atmel announced the AVR32 UC3 core and the UC3 Series A microcontrollers. Atmel is aiming the devices at designers considering ARM's (www.arm.com) ARM7, ARM9, and Cortex-M3 processors. Atmel claims that the UC3 Series A microcontrollers deliver 80 Dhrystone MIPS and consume only 40 mA at 66 MHz when operating from a 3.3V power supply.

The AVR32 UC3 integrates SRAM in a three-stage-pipeline, dual-bank architecture to bypass the system bus to achieve faster execution, cycle determinism, and lower power consumption. An HSB (high-speed-bus)-slave-interface access allows DMA controllers or other HSB masters to write to or read data directly from the closely coupled SRAM. The unit performs arbitration if the CPU and a high-speed slave simultaneously request access, and the priority scheme is programmable to suit application needs. No data hazards exist in the UC3 core pipeline, so the device can update register files during the same clock cycle as instruction execution.

The core is the second that Atmel derived from the AVR32 AP architecture. The 32-bit RISC core has instruction extensions that add DSP instructions to the instruction set of the original core. The DSP instructions include single-cycle MAC (multiply-accumulate) operations covering standard and fractional numbers with and without saturation and rounding and with 32- to 64-bit results. Additional DSP instructions include data-formatting instructions, such as data shift with saturation and rounding.

The ISA (instruction-set architecture) permits freely intermixing 16- and 32-bit instructions. The core shares the ISA as its AVR32 AP parent, with more than 220 instructions available as 16-bit compact and 32-bit extended instructions. Load/store instructions support byte (8-bit), half-word (16-bit), word (32-bit), and double-word (64-bit) data types. The AVR32 ISA has instructions to modify data from the register file before storing it in memory and from memory before storing it in the register file. On-the-fly data manipulations include load-and-insert bit fields, load and swap, and store and swap. The UC3 ISA includes atomic instructions to manipulate mutexes and semaphores and for general bit manipulation.

> The microcontrollers deliver 80 Dhrystone MIPS and consume only 40 mA at 66 MHz.

The core includes power-management functions; a memory-protection unit; and a six-level priority-interrupt controller, including NMI (nonmaskable interrupt) with fast event handling. The core's event-handling system support NMI; exceptions, such as illegal operating codes and bus errors; and four interrupt-priority levels. The first instruction from the event handler executes within 12 clock cycles from an autovectored-handler address. To limit the maximum interrupt latency to 16 clock cycles, pending interrupts can abort multicycle instructions.

UC3 Series A microcontrollers include a peripheral DMA controller, a multilayer HSB architecture, a 10/100-Gbps Ethernet media-access controller, an ADC, two master/slave SPIs (serial-peripheral interfaces), one SSC (synchronous serial controller), a TWI (two-wire interface), four USARTs with hardware flow-control, and full-speed USB OTG (On-The-Go). The microcontrollers are available with an EBI (external bus interface) that extends the addressable physical memory to 16 Mbytes. Its nonmultiplexed, 16-bit data bus can interface to high-density external SRAM; SDRAM; ROM; flash devices; and memory-mapped devices, such as LCDs and FPGAs. The devices include three 16-bit timers and seven PWMs (pulse-width modulators) that can trigger the 10-bit, eight-channel ADC to ease electrical-motor-control design.

The on-chip system manager includes an internal voltage regulator for 3.3V single-power-supply operation, power-on reset, a brownout detector, a hardware watchdog timer, and a real-time timer. The clock system provides an on-chip RC oscillator; two high-frequency external oscillators; one 32-kHz oscillator; and two independent, on-chip PLLs. Special security options are available to protect the flash contents. The device consumes 40 µA in sleep mode and 600 µA/MHz in active mode. You can switch off any section of the UC3 Series A device that is not in use by disabling its clock. The core uses a multithreshold-transistor library to reduce static-power consumption.

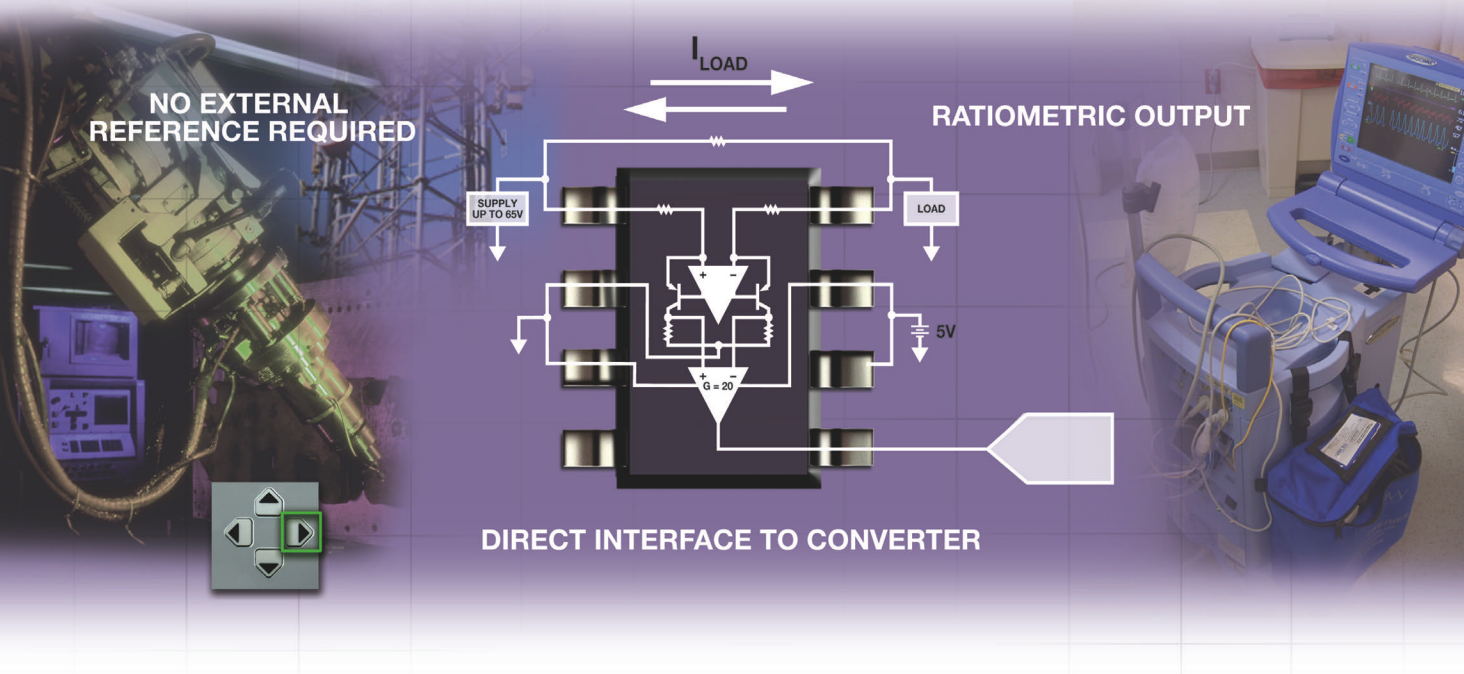
Atmel provides free software, including the GNU gcc C compiler, GNU gdb debugger, FreeRTOS.org real-time kernel, and lwIP TCP/IP (Transmission Control Protocol/Internet Protocol) stack for the family. Atmel's AVR32 Studio and AVR JTAGICE mkII, along with the company's 8-bit AVR microcontrollers, provide the AVR32 UC3 with a multiplatform IDE for the GNU tool chain, including support for more advanced debugging sessions with data and code trace using the AVR32's Nano Trace. The AVR32 UC3 has a Nexus Class 2+ interface through the auxiliary port, providing access to more powerful debugging features, including nonintrusive data and program trace. The EVK (evaluation kit) 1100 is available to support the devices. It includes Ethernet and USB interfaces, as well as SPI, TWI, and USART serial-communications ports. A 20×4-character LCD and the expansion connector allow advanced product evaluation and prototyping activities.

The two first devices of the UC3 Series A are available for sampling now and will be available in volume production in the fourth quarter of 2007. The AT32UC3A0512, with an EBI and 512 kbytes of flash, is available in a QFP144 for $8.16 (10,000). The AT32UC3A1512, without an EBI and 512 kbytes of flash, is available in a QFP100 for $7.43 (10,000).

—by Robert Cravotta

▷**Atmel**, www.atmel.com.

Bidirectional current monitors that make sense.
In measurement and control, analog is everywhere.



AD8210
Bidirectional Current Sense Amplifier

- –2 V to +65 V operating common-mode voltage range
- –40°C to +125°C operating temperature range
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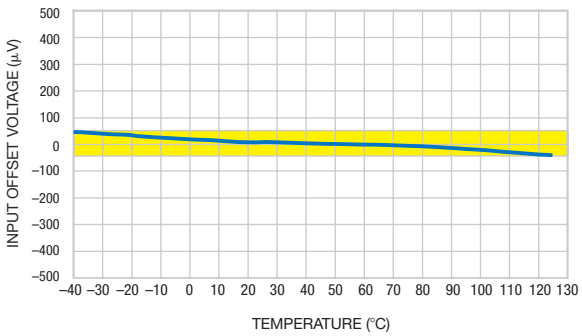
- 10 ppm/°C typical gain drift
- Gain of 20
- 500 kHz bandwidth
- Price: $1.79/1k

Typical ≤ 1 µV/°C Offset Drift



Precision over temperature—guaranteed

With our new AD8210 bidirectional current sense amplifier, you get the industry's most integrated, flexible, and accurate current sense monitor. With features like ±8 µV/°C maximum offset drift and 20 ppm/°C maximum gain drift guaranteed across the entire –40°C to +125°C temperature range, it represents a milestone in precision current sense monitoring. The AD8210 improves your ability to meet your error budget and to control more precisely a wide range of loads in communications, industrial, and medical applications. Two other bidirectional monitors—the AD8205 (gain of 50 V/V) and the AD8206 (gain of 20 V/V)—offer 50 kHz operation and excellent performance over temperature.

All three amplifiers feature an innovative ratiometric output offset architecture that inherently improves the accuracy of your ADC and your system. With a typical 5 V single-supply, each device can be configured for both bidirectional and unidirectional current sensing. Excellent output accuracy is maintained throughout the input voltage range through the use of a proprietary thin film precision network.

For more information on ADI's current sense amplifiers and monitors, please visit *www.analog.com/currentsense* or call 1-800-AnalogD.

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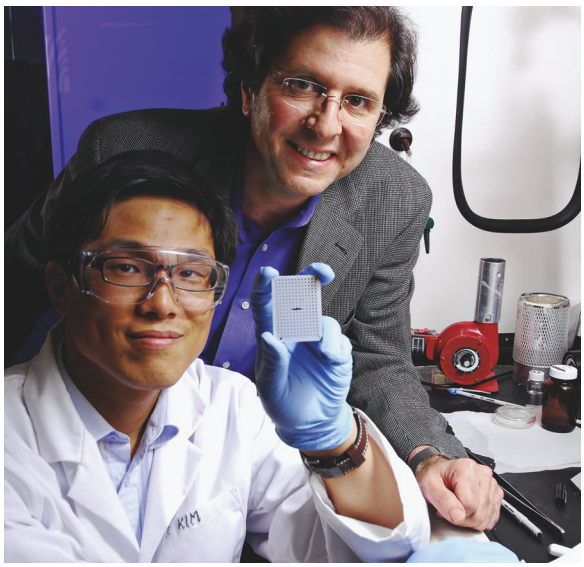
ANALOG DEVICES

RESEARCH UPDATE

BY RON WILSON AND MATTHEW MILLER



Researcher Philseok Kim (left) and Professor Joseph Perry (right) display a capacitor array fabricated using a new nano-encapsulated dielectric material.

Nanocomposites promise advance in thin-film electronic components

Research at the Georgia Institute of Technology Institute for Organic Photonics and Electronics has demonstrated a technique for using nanofabrication principles to employ a powerful, but hitherto intractable, dielectric material in thin-film capacitors and, potentially, transistors. The material, barium titanate, has long been known to have a high dielectric constant. But the substance tends to clump when suspended in a polymer, creating large granules that exhibit very low breakdown voltage.

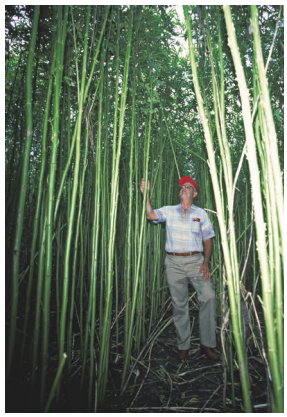
The Georgia Tech team, led by Professor Joseph Perry, tried nano-encapsulation to tame the clumping and create a uniform dispersion of the barium titanate in the polymer matrix. To achieve this goal, Perry's team turned to a second group, led by Professor Seth Marder, to synthesize a designer phosphonic-acid ligand that would both bond securely to the barium titanate and form a capsule compatible with commonly used thin-film polymers. The resulting capsules range from 30 to 120 nm in diameter, as much as four times smaller than granules researchers have fabricated using conventional means. The smaller encapsulated particles also proved friendly to the host polymers, achieving uniform dispersion and hence yielding thin-film capacitors with as much as twice the capacitance per unit area of previous attempts. Perry sees further application in gate dielectrics for thin-film field-effect transistors.**—RW**

▷**Georgia Institute of Technology**, www.gtresearchnews.gatech.edu.

NEC plastic cools the palm and the earth

A new carbon-fiber-enhanced plastic material from NEC Research has the potential to both more evenly spread heat in the enclosures on electronic devices, such as cell phones, and to help global warming. The material is made from more than 90% biomass material; you can't get much greener than that.

The material is formed using a specially developed binder—literally, a secret sauce—in a PLA (polylactic-acid) resin. The action of the binder causes carbon fibers suspended in the resin to cross-link, forming a web of heat-conducting fibers. When formed into the case on an electronic device, such as a cell phone, this cross-linked web conducts heat laterally, away from hot spots on the package, as well as vertically, through the case, at rates in excess of the conductivity of stainless steel. Thus, the package can cool itself without causing uncomfortable hot spots on the surface above heat-generating components.



The kenaf plant may be the future of plastic enclosures for handheld electronics.

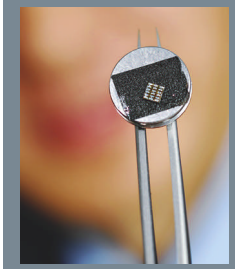
The material's green credentials are impeccable. NEC is making the PLA resin—a polymerized lactic acid—by fermentation of kenaf—a super-fast-growing, carbon-dioxide-voracious African/Asian plant related to cotton. NEC researchers have succeeded in getting the kenaf-derived PLA to have good molding properties, high heat resistance, and compatibility with the company's special binder.**—RW**

▷**NEC**, www.nec.co.jp/rd/rel/english/topics/t38.html.

ENERGY HARVESTER GENERATES CONTINUOUS NANOAMPERE CURRENT

05.24.07

Researchers at the Georgia Institute of Technology have created a tiny device that produces a direct current by harnessing the piezoelectric output of hundreds of swaying zinc-oxide nanowires. Buffeted by ultrasonic waves or mechanical vibration, the device features a forest of vertically oriented nanowires, whose tips lie in the valleys of a peak-and-valley-shaped electrode. As the wires flex, they periodically contact an electrode and transfer their electrical charge. A prototype device produces current in the nanoampere range, but the researchers claim the technology can scale to produce 4W/cm³.—MM



A tiny device produces a direct current by harnessing the piezoelectric output of hundreds of swaying zinc-oxide nanowires.

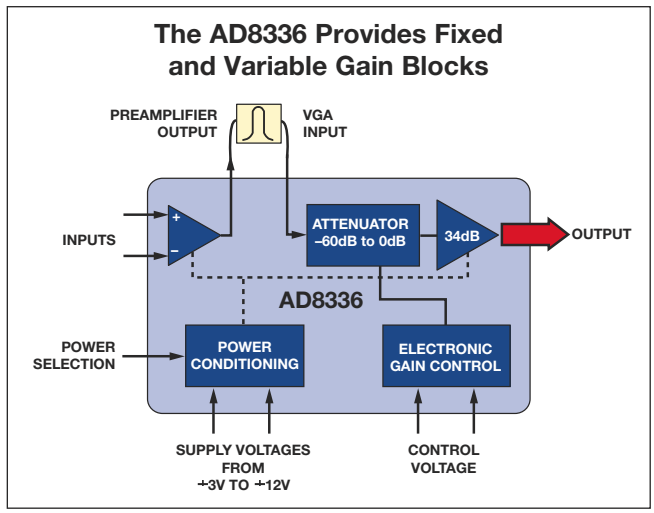
▶Georgia Institute of Technology, www.gatech.edu.

LEADING inside

A series of engineering insights by Analog Devices.

Solving Dynamic Range Problems in Analog Systems

Many of the applications that we take for granted operate in real-world environments with high levels of dynamic range. The most common of these systems are radio and television receivers and their updated cousins—the cell phone and the iPod. The signal range for these types of household devices can vary from a few microvolts in remote areas to volts when the device is near the signal source. Situations with wide dynamic range are also found in scientific, industrial, and medical applications—such as the "front ends" of measurement equipment, ultrasound imaging for biological diagnostics, and industrial fault analysis. Designers have been faced with the dual challenges of providing the highest sensitivity amplifiers possible while at the same time making them operable under severe overload conditions.



In the early days of electronics, solutions to these challenges were sought by "tinkering" with the amplification devices. In the case of vacuum tubes, this involved adding control grids within the tube structure to alter the conductivity and thus, the gain of the device. For transistors, electronic gain control was limited to adjusting the dc base or emitter currents. While these solutions were relatively successful, they typically compromised linearity and distortion performance. A more viable solution had to wait until the advent of highly complex integrated circuits in the late 1980s, when Analog Devices invented and introduced the AD600—the first solid-state variable gain amplifier (VGA) to operate in a linear manner.

This amplifier was also called the X-amp or exponential amplifier. The advantages of this device lie in its architecture—a passive electronic gain control implemented with a resistive ladder network and followed by a fixed-gain amplifier. There are six to eight "rungs" on the ladder, connected to an "interpolator circuit" that sweeps across the ladder in response to an externally supplied control voltage. This concept has been the basis for many subsequent products that offer additional features and enhanced performance. However, the basic gain-control architecture has not changed.

The AD8336 is one of several newer solutions in Analog Devices' VGA portfolio. This device offers an industry-leading balance of size, performance, and circuit versatility while operating across wide power supply voltage and dissipation ranges.

The versatile AD8336 variable gain amplifier features an uncommitted, fully independent voltage feedback op-amp to which ac- or dc-coupled signals of either polarity can be applied. The preamplifier output can be applied directly to the VGA input—or interstage selectivity or filtering can be inserted between the preamplifier and VGA. The preamplifier can be connected as a summing stage or differentially like any high frequency op amp—enabling fast, convenient interconnection to virtually any signal source.

Just as the preamplifier is capable of differential connections, so too is the gain control input. The input may be ground referenced or connected from a reference supply appropriate to the gain control source. This capability is particularly useful with cascading devices. For higher voltage applications, the device may be operated from supplies as high as ±12 V or as low as ±3 V for battery operation. To conserve battery life, the power may be reduced by approximately 50% at the expense of bandwidth.

Analog Devices offers an extensive portfolio of variable gain amplifiers for applications such as ultrasound, radar, and wireless communications. For data sheets, free samples, and additional information, please visit *www.analog.com/LI-VGA* or call 1-800-AnalogD. ▶

Author Profile: ***James Staley*** *is an applications engineer in the Integrated Amplifier Products Group at Analog Devices.*

BY HOWARD JOHNSON, PhD

In-between spaces

I measured the inductance of four loops of wire. Each loop comprises the same length of insulated #10 AWG solid-copper wire (**Figure 1**). During testing, I probe the wires at their endpoints (bottom of **figure**), holding the wires vertically above the tester and well away from all other metal objects.

The leftmost loop, the round one, has a diameter of 10 in. It gives the largest inductance at 730 nH. Moving to the right, the inductance drops in each case until you reach the final loop, the twisted wire, at 190 nH.

I mention this simple experiment because I have all too often heard engineers say: "My via has an inductance of 1 nH," or "My bypass capacitor has an inductance of 500 pH." Those statements assume that you can ascribe discrete inductances to individual portions of a signal path.

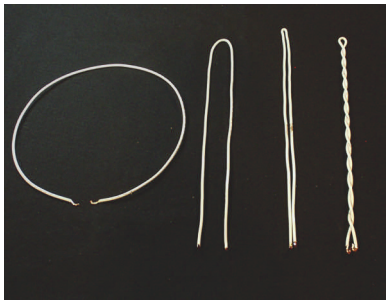


Figure 1 Each loop of wire is the same length, yet they each have inductances, from left to right, of 730, 530, 330, and 190 nH.

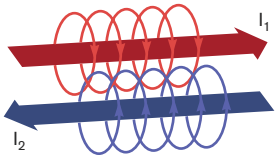


Figure 2 Magnetic fields from the outgoing current (red) nearly cancel the equal-but-opposite magnetic fields from the returning signal current.

That assumption is a good one when dealing with macroscopic components. According to Kirchhoff's laws for circuit analysis, the total inductance of two inductors in series should equal the sum of their independent inductances.

The correctness of Kirchhoff's analysis hinges upon a crucial precondition, namely that no significant electromagnetic fields inhabit the spaces between conductors. High-speed digital currents infuse the spaces between conductors with massive, fast-changing electromagnetic fields. These digital circuits do not meet Kirchhoff's precondition; therefore, Kirchhoff's laws are invalid in the high-speed domain.

In high-speed electronics, you must supplement Kirchhoff's laws with parasitic capacitance, due to electric fields, and parasitic inductance, due to magnetic fields.

Figure 2 illustrates the pattern of magnetic fields surrounding two wires. The wires carry equal and opposite currents, much like the hairpin structures in **Figure 1**. Imagine current I_1 going out on one wire, changing direction at a hairpin turn, and returning as I_2 on the other wire.

If you observe from a remote distance, the magnetic fields that I_1 generates nearly cancel the equal-but-opposite magnetic fields that I_2 generates. The closer you bring the wires, the better the cancellation, and the smaller the overall magnetic-field energy.

Inductance L represents nothing more and nothing less than the total magnetic-field energy, E, surrounding a current-carrying circuit. The precise relation between inductance and field energy is:

$$E=\frac{1}{2}LI^2.$$

If the spacing between wires affects the stored magnetic energy, then the spacing affects the circuit inductance, as well.

This interaction between magnetic fields explains why you cannot ascribe inductance to one part of a distributed circuit without also specifying the shape and location of the complete signal-current path. It might increase or decrease the inductance. All parts of the path influence the inductance.

For example, the inductance of a via depends on the location of nearby interplane connections. The inductance of a bypass capacitor depends on its proximity to the reference planes.

Inductance is not a property of an individual component. In distributed circuits, inductance is a property of the spaces between conductors. EDN

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Howard Johnson, PhD, of Signal Consulting, frequently conducts technical workshops for digital engineers at Oxford University and other sites worldwide. Visit his Web site at www.sigcon.com or e-mail him at howie03@sigcon.com.

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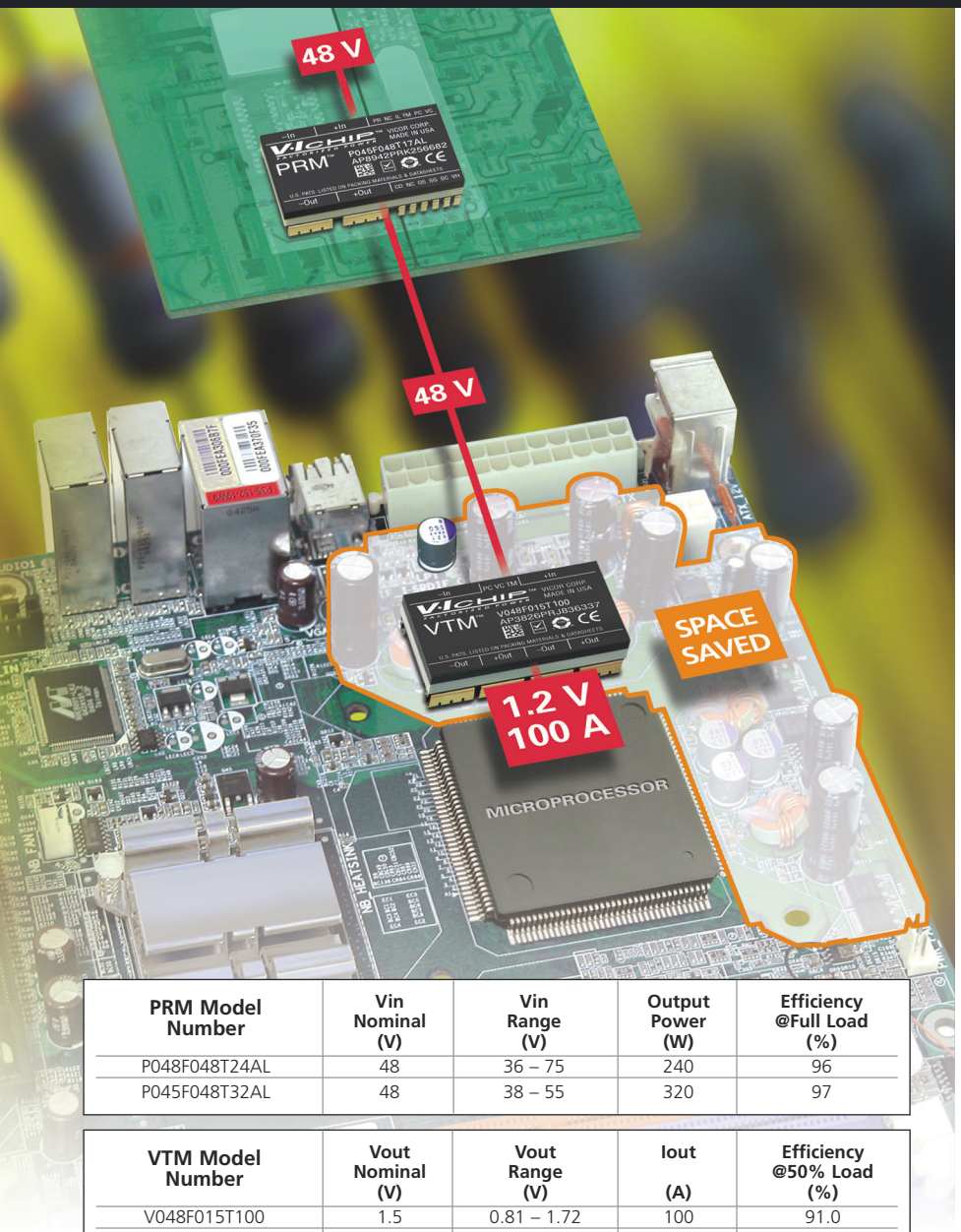

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BY JOSHUA ISRAELSOHN, CONTRIBUTING TECHNICAL EDITOR

Confer for continuing education

Early in this decade, popular wisdom had it that professional conferences in the electronics industry were going the way of the dodo bird. Internet Web sites, videoconferencing, and e-mail would put live events out of business.

So much for popular wisdom: Despite the high cost of jet fuel and the high impedance that governments present to air travelers, attendance appears robust at the better professional conferences in our field. For example, this year, the ISSCC (International Solid-State Circuits Conference) attracted a nearly record-breaking attendance of more than 3600. APEC (Applied Power Electronics Conference and Exposition) *did* break its attendance record with nearly 2800 attendees from 32 countries and more than 1000 organizations.

More important than the numbers, the conference experience is rich, particularly for those of us who are interested in analog and power technologies. Both conferences are IEEE affiliates and are duly famous for the quality of their paper presentations, which make up their schedules' core. Strong educational programs, less-formal panel discussions, and *rap sessions* complement the paper tracks and give attendees opportunities to learn from and interact with peers and leaders in technical innovation.

Though the conferences take different approaches to organizing and presenting their educational programs, educational sessions at both events were at or near capacity this year. I haven't space to fully describe these offerings—see www.isscc.org/isscc/ and www.apec-conf.org for more information and announcements of 2008 events—but I'd like to point out one series from each.

[Rap sessions] usually start with position statements from each member of the panel but ... rapidly devolve in formality and evolve in depth and breadth.

ISSCC offered 10 two-hour tutorials scheduled so that attendees could choose as many as two. Attendees received prints of the presentation slides for the sessions they attended and prices were à la carte. Of the 10 tutorials, eight featured analog topics. The strong analog component does not indicate that the ISSCC ignores digital technologies and design challenges. On the contrary, some of the most vexing problems digital designers must face, particularly when designing for 90-nm and smaller process nodes, derive from the awful reality that digital, though a useful abstraction, is only that: Increasingly, analog effects deriving from fundamental physics limit the performance of digital topologies.

APEC's professional-educational-seminar program comprised 18 three-and-a-half-hour sessions in three blocks. In contrast to the ISSCC's à la carte approach, APEC offers its seminars as a package. Attendees receive the printed slides for all 18 seminars—nearly 2000 in all—and can attend any session they wish without declaring their preference in advance. APEC charges nearly three times the ISSCC's single-session price, which does make negotiating the expense with one's organization a bit tougher. However, the ability to peruse the slides from all of the presentations allows attendees to better compare and assess the value of competing sessions.

Both conferences schedule evening panel discussions or rap sessions. These sessions usually start with position statements from each member of the panel but, with luck and audience participation, rapidly devolve in formality and evolve in depth and breadth. Standouts this year included "Digital RF—Fundamentally a new technology or just marketing hype?" at ISSCC, which Stanford University Professor Thomas Lee moderated, with panelists from UCLA, Infineon, Intel, Texas Instruments, Hitachi, and Silicon Labs, and "If it ain't broke, why go digital?" at APEC, which Darnel Publisher and President Jeff Shepard moderated, with panelists from Microchip, Primarion, Coldwatt, Maxim, and Tyco. Ironically, though the titles of both sessions suggest digital topics, discussions largely centered on analog effects and realities. More surprising was that though power and RF are literally opposite ends of a spectrum, both sessions hit upon a few topics in common. EDN

Contributing Technical Editor Joshua Israelsohn writes about analog and power applications and technologies. Contact him at jisraelsohn@ieee.org.

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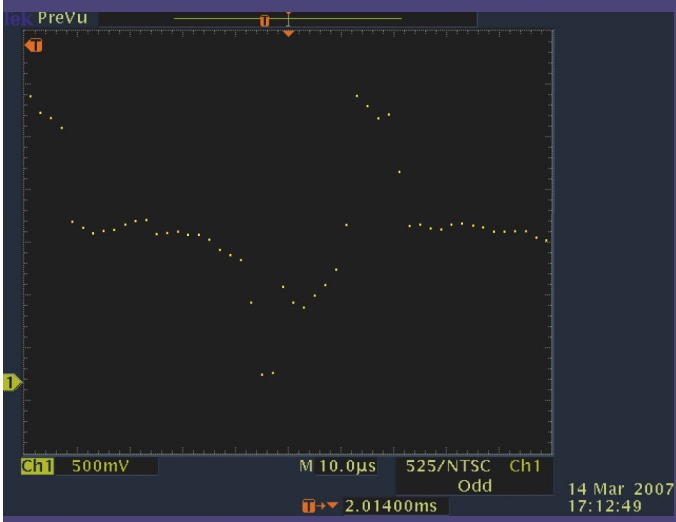

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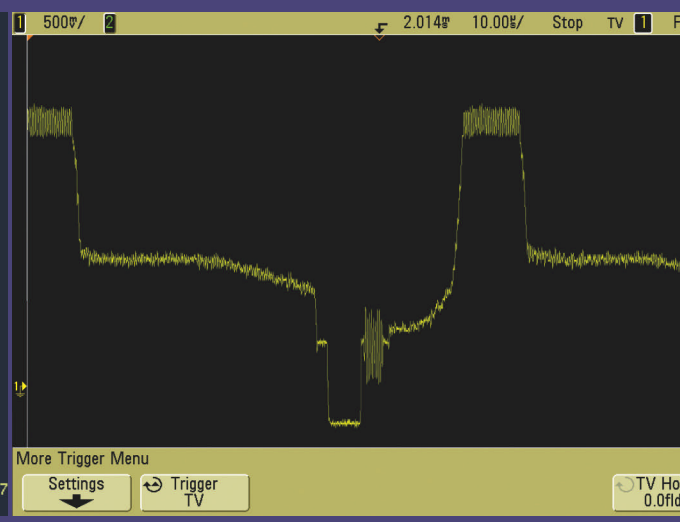

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**Tektronix TDS3000B Series User Manual 071-0957-04, October 4, 2004.*
***Agilent 5000 Series Oscilloscope data sheet, Pub No 5989-6385EN, April 18, 2007.*
Agilent and Tektronix oscilloscope acquisitions taken at identical settings: horizontal timebase = 2ms/div, vertical volts/div = 500 mV/div, connect the dots = on. 10:1 passive probes used for both measurements. Final screen images show both acquisitions zoomed in to 10 µs/div.

Agilent Technologies

BY REED P TIDWELL • XILINX

The power of the hot seat

DANIEL VASCONCELLOS

In the mid-1980s, I was designing visual systems for flight simulators for computer-graphics company Evans & Sutherland. These systems were huge—dozens of 19-in. racks full of cards working together to produce the out-the-window cockpit scene. The primary technologies were wire-wrap and 74LS logic. One of these big, multimillion-dollar systems was ready to ship to NASA, but, two days before the ship date, final testing turned up "sparkles" in several visual channels.

The only obvious thing was that the problem originated in the display processor, a collection of about 100 wire-wrap boards and PCBs (printed-circuit boards) plugged into a wire-wrap backpanel. To make matters worse, this system had 1024×1024-pixel resolution, which required four display processors load sharing in the scan-line-interleaved fashion that some commercial graphics chips now use. Thus, the potential offenders included about 400 cards, probably 100 cables, and hundreds of thousands of wire-wrap wires.

Management assigned me to find and fix the problem. We found that the picture from each individual processor was good on its own, but the combined image possessed the dreaded sparkles. The chief suspect became the fastest clock in the system, which had a blazing 25-nsec period. (Most clocks were 100 nsec.) This clock, which was the basis of all the frame-buffer output and video timing, crossed wire-wrap backpanels eight times, traversed wire-wrap cards 16 times, and traveled through three ribbon cables, with the system rebuffing it several times along the way. By the end, it looked awful.

I figured that a good approach might be to use ECL and differential signaling to control rise and fall times and reduce common-mode noise. Fortunately, we had a handful of parts available and a built-in −5.2V power supply. Unfortunately, doing the conversion at this late date meant mass rework to get new power to some cards, placing new parts on many cards, and replacing lots of single wires with twisted-pair wires. Nevertheless, from my position in the hot seat, I had almost every company resource at my disposal.

Consequently, our team reworked and tested one processor. The clock looked clean, so we reworked the other three processors in the channel. In the combined system, to our distress, there were severe anomalies in the last processor. We found that, although the clock was clean, its duty cycle was distorted to the point that it was just a thin pulse. Going back to the data book, I learned that the rise time of ECL is typically 0.5 nsec slower than the fall time. Each of the buffers was eating away at that 12.5-nsec high time of the clock. Inverting the clock at strategic points restored balance to the duty cycle and vanquished the sparkles.

I explained the issues and the solution to management. Initially, there was some resistance due to the amount of rework involved. However, I soon had support up and down the chain of command. We completed the sign-off process, which normally took weeks, in hours. Subsequently, a small army of rework technicians attacked the remaining dozen or so processors. As each channel was completed, the technicians would fire it up, verify that it was sparkle-free and still worked, and then wrap up the racks and take them to the loading dock. We started shipping the product on the day it was promised.

Aside from signal-integrity insights, the most valuable lesson I learned was organizational: Though the hot seat is uncomfortable, it bestows unique power to cut through red tape. EDN

Reed P Tidwell is a senior staff applications engineer for the Advanced Products Division of Xilinx. Like Reed, share your Tales from the Cube and receive $200. Contact Maury Wright at mgwright@edn.com.

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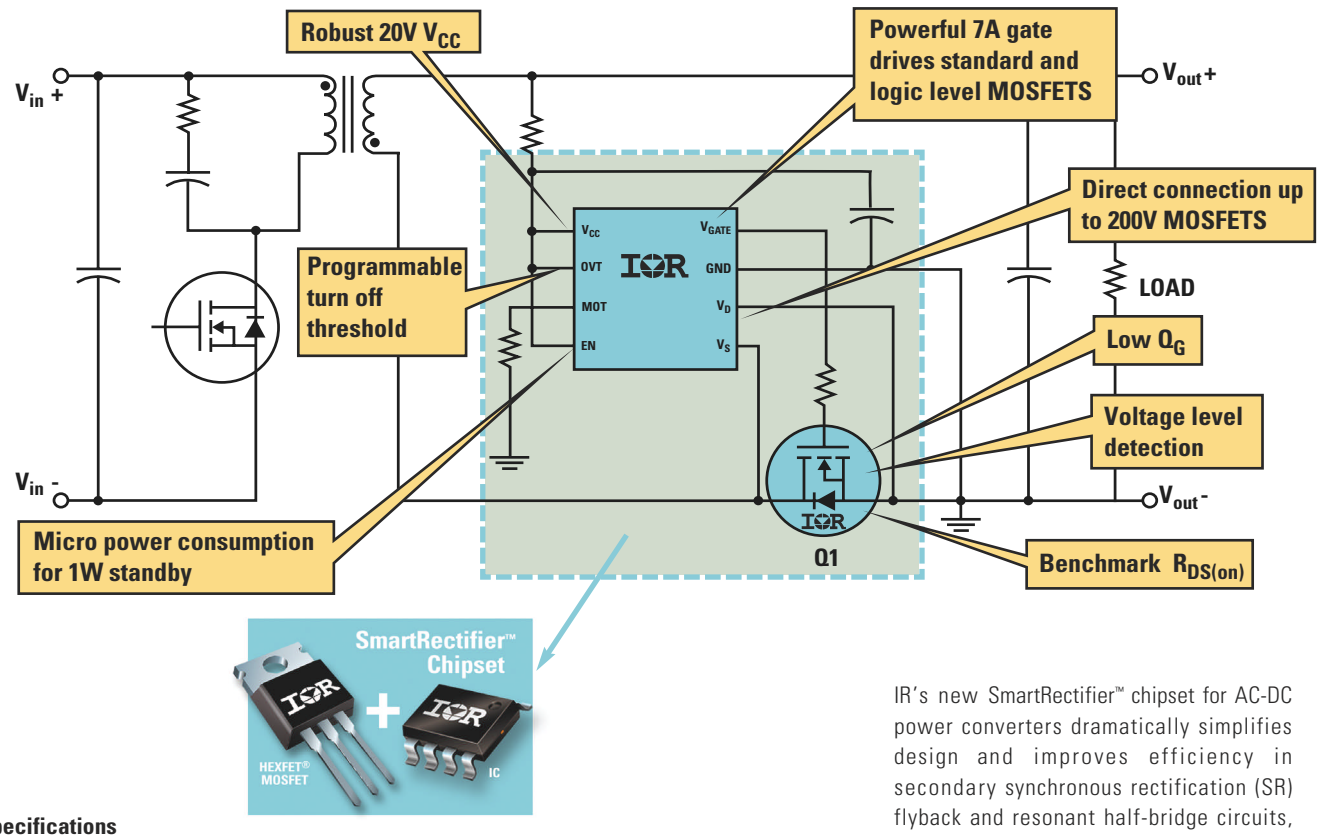

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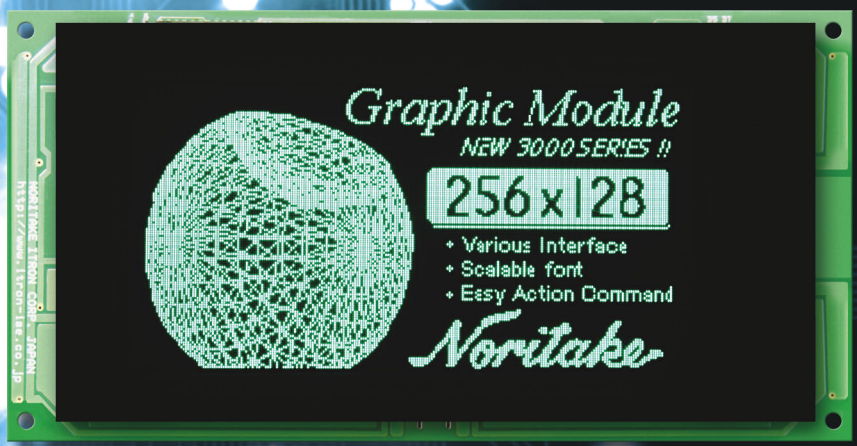

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CMOS IMAGERS ENABLE MANY CHOICES, FROM CAMERAS ON CHIPS TO DISTRIBUTED-PROCESSING ARCHITECTURES, BUT THE WILD CARD MAY BE AUTOFOCUS TECHNOLOGY.

BY RON WILSON • EXECUTIVE EDITOR

Compact imaging systems face partitioning issues

The triumph of CMOS-image-sensor technology over CCD (charge-coupled-device) sensors has opened a world of new options to camera designers, especially in the midrange-DSC (digital-still-camera) and cell-phone-handset markets. CCD-process technology sufficiently differs from CMOS-logic processes so that the only feasible configuration for a CCD-based imaging system is a stand-alone sensor chip that connects to separate digital-image-processing hardware. With CMOS sensors, however, the image-sensor array may be on the same die with as much mixed-signal and digital content as the designer cares to pay for.

This situation has opened the door to a genuine camera on a die, with light entering and JPEG files exiting. But that scenario is just one of the alternatives. Examining the partitioning decisions camera designers are making today reveals a wealth of detail about how these systems work. It also offers a case study in system partitioning that applies to many other highly integrated systems. And it gives a peek into an emerging technology that could change almost everything about the way miniature cameras function.

THE IMAGING CHAIN

Figure 1 depicts the first chapter in this story: the image-processing pipeline as most camera designers understand it. The first item of interest in the pipeline isn't electronic at all. It is the objective lens. Today's lenses for handsets and small DSCs are children of computer-aided optical design and the crushing demand for compactness in shirt-pocket handsets. The need to make the lens as short, light, and inexpensive as possible has led to designs radically different from those that cameras used a decade ago. It has also led to the use of severely compromised lenses that require intensive digital image processing to correct their deficiencies. As you'll see later, this development has been the seed for an important innovation.

The function of the lens is to focus an image onto the surface of the sensor. Less obviously, that function also includes varying the point of focus to adjust for subject distance; varying the amount of light reaching the sensor; and, in a zoom lens, varying the effective focal length of the lens to create a wider or narrower field of view. Today, camera manufacturers perform all of these functions by electromechanical means, which algorithms farther down the pipeline generally control.

Another cluster of optical devices lies between the objective lens and the sensor. In many designs, a microlens covers

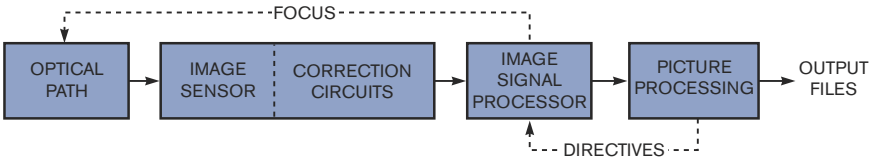

Figure 1 There are many ways to partition the functions in a digital imaging system, but the stages in the pipeline remain similar and maintain the same order.

each pixel in the sensor array; this lens gathers a large portion of the light striking the pixel and directs it onto the PIN diode. Beneath this lens, every color-imaging array except one has a set of color filters, usually in triplets of red, green, and blue. This setup allows the sensor to distinguish colors, but it also divides the raw resolution by a factor of approximately three. And it reduces the amount of light actually reaching the sensor.

The next item in the list is the sensor itself: a rectangular array of pixels. Each pixel contains a photosensitive diode that allows charge to flow onto a capacitive node roughly in proportion to the amount of light striking the diode. Three or four transistors generally reset the cell, allow sampling of the capacitor voltage on the sense line, and reduce leakage. As in a DRAM array, the transistors route the small voltage on the capacitive node onto a bit line and thence to a sense amp. But, unlike in a DRAM, this voltage has analog meaning, so the fidelity with which the amplifier senses it directly contributes to image quality.

The next block in the **figure** is the correction and conversion circuitry. Much of the noise on the sense lines is predictable based on the location of the pixel and the timing of the circuit. Great effort goes into backing this noise out of the signal. An amplifier and a data converter complete this stage, rendering the light striking the pixel during the shutter interval into a digital quantity.

This string of digital data goes to the next block—frequently, a separate ISP (image-signal-processor) hardware module—for pixel-level processing. Here, algorithms can improve the image on a pixel-by-pixel basis by performing such tasks as color correction—to compensate for the "off" color of artificial illumination, for instance—and to correct overexposure or underexposure problems. The output of this block is a raw stream of pixels with simple manipulations to make the image look accurate.

From there, the image goes to what you might term image-level processing, during which the image undergoes more complex manipulations that require working on larger amounts of data. For instance, algorithms might identify and remove "red eye," or they might correct for the vignetting and barrel distortion from a cheap lens.

More dynamic actions can go on here, as well. Algorithms can at this point analyze the image to provide commands to the autofocus motor. In DSCs, other algorithms may perform pattern recognition to classify the image—portrait, scenic, or close-up, for instance—and to extract features for further image enhancement.

AT A GLANCE

- CMOS-imager technology makes possible many partitioning options, from multichip boards to camera-on-chip designs.
- Process technology, physical limitations, culture, and politics all play roles in these partitioning choices.
- A new technology, EDOF (extended depth of focus), could change not only digital cameras, but also the way designers make partitioning decisions.

PARTITIONING DECISIONS

It is rare for each block in the pipeline to reside on a separate chip, although this case may be true in high-end DSCs. The range of partitioning choices stretches all the way from such multichip systems to a single chip containing all the blocks in the pipeline. A number of factors intertwine to help architects find their place within this domain. These factors include physical limitations, boundaries of IP (intellectual-property) ownership or design-team competence, and the influence of underused—or overstretched—resources elsewhere in the camera. Interacting with these broad influences are implementation decisions, such as algorithm choices, process-technology decisions, and company politics.

The most clearly defined parameters of the partitioning decision are physical limitations. Some of these involve packaging. A wall-mounted security camera plugged into a 240V outlet may have few or no packaging restrictions. A clamshell handset in which the entire camera is supposed to reside in the flip-up cover lives at the other extreme. "The phone market is all about the X, Y, and Z dimensions," says John Gerard, vice president of marketing at MagnaChip. "Not only is there no room for several chips, there is often not enough vertical clearance for a stacked multidie package." Such restrictions bias the design toward a single chip, such as those that MagnaChip currently offers (**Figure 2**).

Algorithms also play a key role in single-die approaches, because of SRAM. "Sensor-oriented CMOS processes don't always support the best SRAM," observes Daniel van Blerkom, chief technology officer at Forza Silicon. "That limits the amount of SRAM you can have on an affordable die, and that, in turn, limits the amount of image-processing work you can do on the die. I

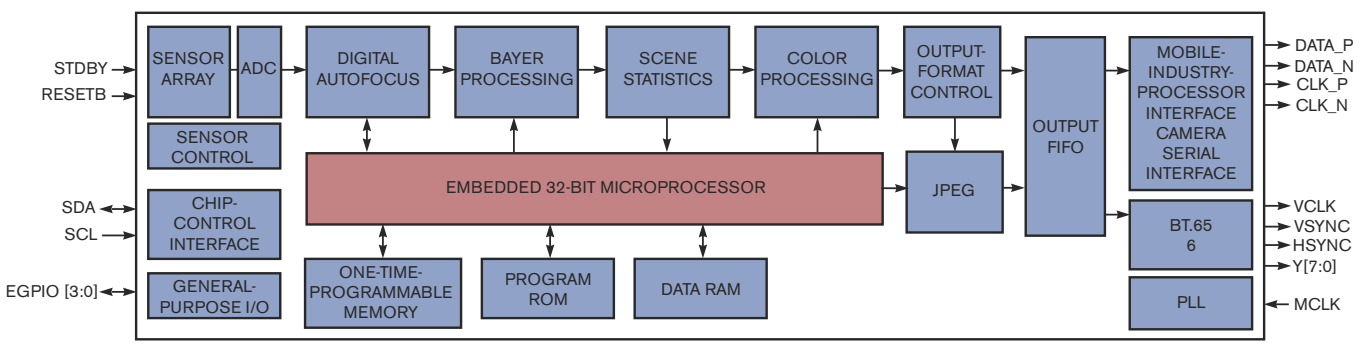

Figure 2 The MagnaChip 531 Ex integrates a 3.2M-pixel sensor array with a full image-processing subsystem on a single die.

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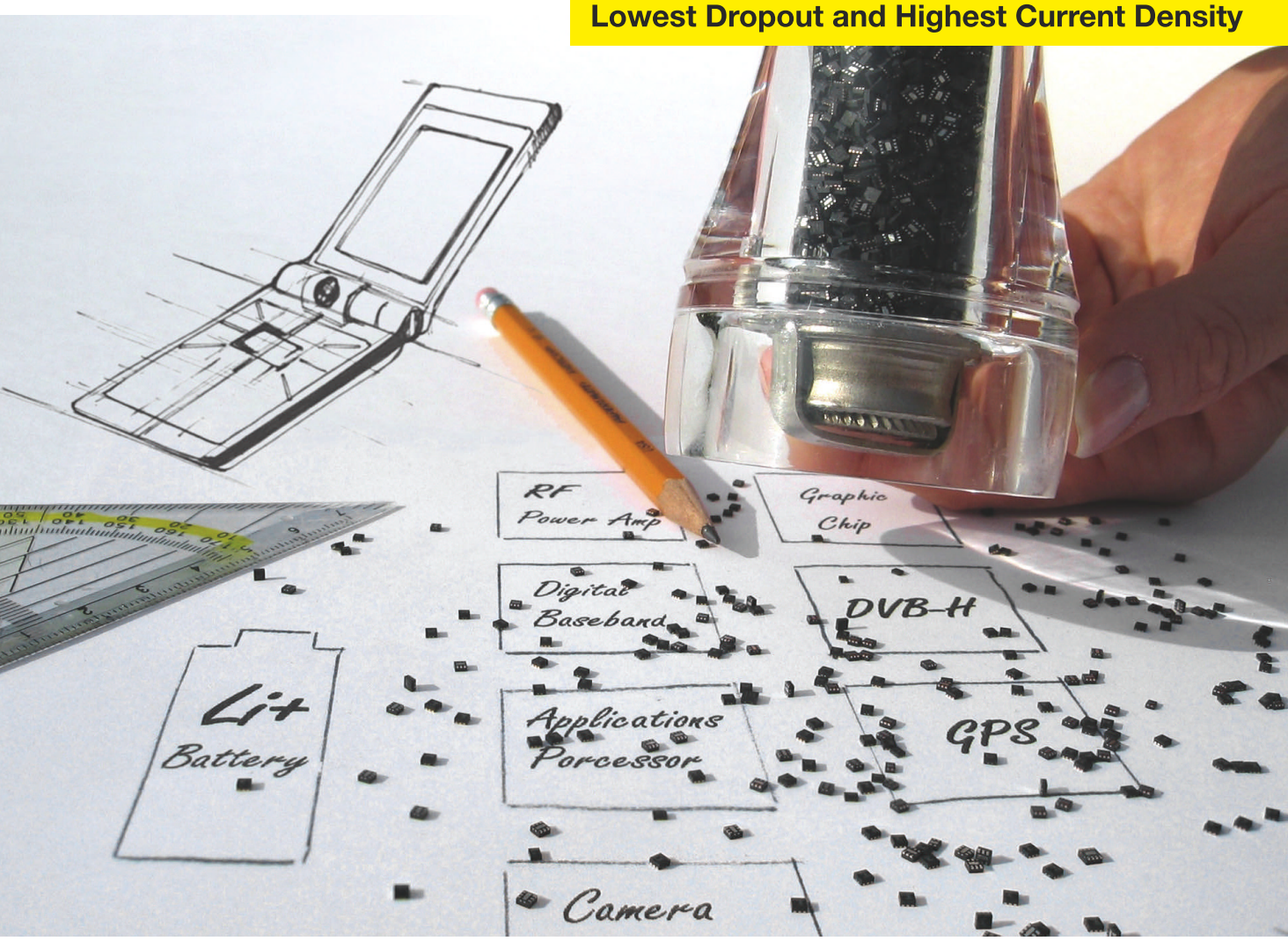

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have yet to see an imaging chip with an on-chip frame buffer."

Gerard agrees: "If you have algorithms that require a full frame of data, you need a multichip solution," he says.

The question of algorithm design closely links to memory and processing requirements. Clever designers have found that, using just a few lines of data, they can do many techniques on the fly that photo kiosks might apply to a full image. "A high-end DSC may have several frame buffers for different functions," says Sandor Barna, director of strategy and planning at Micron Technology's imaging operation. "But without that kind of memory space, you have to use algorithms that make decisions based on statistics you've collected over a few previous frames."

Barna says that such algorithms can be ingenious. "For instance, with a frame buffer you can do quite sophisticated correction for camera shake. Without it, you can still monitor the data stream for motion and capture the image at an instant when the motion is least. Or, you can just recognize that camera shake is going to be an issue and increase the shutter speed." Similarly, whereas a DSC might gather data from a full frame to establish exposure and white balance, a handset camera module might approximate this data by accumulating average luminance and chrominance values on the fly as pixels flow through the chip in preview mode.

THE QUESTION OF ALGORITHM DESIGN CLOSELY LINKS TO MEMORY AND PROCESSING REQUIREMENTS.

Another physical limitation—over which there is much more debate—is the matter of optimization for the sensor elements. This issue tends to be almost religious and deeply embedded in the origin of a company. Micron Technology, for instance, with roots in DRAM design, argues in favor of an inherently low-leakage process. "The industry is gradually converging on a process that combines low leakage—to preserve the charge on the pixel until you can read it out—with good logic density," says Barna. "It has been a great help to us to have started out from a DRAM background, because leakage is directly related to wafer contamination—something DRAM people have had to deal with much more carefully than have logic-process people."

Companies such as Toshiba, coming from primarily a logic business, see just the opposite. "Leakage from the photodiodes is not an ideal problem to have. Everyone has to address it," says Andrew Burt, vice president in Toshiba's imaging-marketing group. "We take the approach

A BRIEF EXPLANATION OF EDOF

The technology behind EDOF (extended depth of focus) is not intuitively obvious to most engineers unless they have been involved in physical optics. So, perhaps some explanation is in order. This one follows a discussion with Arie Shapira, director of sales engineering at EDOF start-up Dblur Technologies Ltd.

In a conventional optical system, the lens focuses the light wavefront arriving from each point in the scene onto a single corresponding point in the image–in the case of digital cameras, on the surface of the image-sensor array. If the light from a point in the scene is smeared over a diffuse area instead of contained within a point, the lens is out of focus, and the image is blurred. This blur is not random. The lens transforms a point source into a blur through a mathematical transform called a point-spread function, Shapira explains. You can think of it as the 2-D impulse response of the lens.

As a transform, the blur can be reversible. Under some conditions, digital-signal processing can reconstruct a sharp image from the superposition of all the blurred images from all the points in the scene. It is a small matter of an inverse 2-D transform, which you can implement with a 2-D convolution. This method works if the sensor is fairly linear and the point-spread function is well-behaved. Anyone who has used Photoshop's unsharp mask to fix up their digital-camera images is aware of the idea.

Now for the fun part: You can design a lens that is intentionally out of focus, so that it creates a blurred image from a point source all the time and–this part is cricital–so that the point-spread function is nearly independent of how far the point source is from the lens. So, if the points in the scene are on the surface of a business card 10 cm away or if the points are on the side of a building 100m away, you get the same kind of pattern in the image.

When the reconstruction algorithm transforms those individual blurs back into nice, sharp points, the inverse transform is still independent of the distance between subject and lens. The business card close to the lens is in focus, and so is the building. You have extended the depth of focus far beyond that of a conventional lens. You can use the technology in other ways, as well: to control known aberrations in the lens, for instance, or to increase the optical system's tolerance for mechanical inaccuracies.

Key to this technology is that you must design the lens and the reconstruction algorithm together Shapira emphasizes, so that the lens performs the same spatial transform that the image processor inverts. So, the lens and the software must match. Necessarily, losses occur in the process, so it is just as important that the lens and sensor be able to deliver image quality in excess of what the user expects. In this way, the resulting image, after reconstruction, will meet the user's needs.

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of starting out with a digital-CMOS process, which gives us enormous efficiencies of scale, and doing intensive pixel design work to get the performance of the array to where we want it."

Another issue with its roots in process technology is the ability to manage noise. "Noise becomes a nightmare for designers as the pixel pitch gets down to 1.5 microns, says van Blerkom. "As the pixels get physically smaller, the analog designer works much harder." Designers use multiple-well isolation, physical guard rings, and luck to try to keep digital noise out of pixels that give up more and more margin in the name of larger pixel counts. Designers complain of a lack of sufficiently accurate substrate models for charge injection from the digital circuitry and that the entire imaging array is often poorly modeled. So, conservatism and test chips provide the best insurance.

IP BOUNDARIES

Technology aside, the source and nature of the IP in a block may set partitioning decisions. This influence is most clear in some handset OEMs that want nothing to do with the design of the camera module. "Some OEMs just want to feed in power and clock and get back files," says Michael de Luca, marketing manager at Kodak. "But some of that may just be immaturity in the market. In principle, there is probably a best partitioning for a given set of end-user needs, and it requires some involvement by the phone manufacturer."

Still, there are some natural IP groupings. For instance, virtually everyone acknowledges that sensor manufacturers should perform corrective processing and data conversion to generate digital raw-pixel data because they know the peculiarities of their sensors. After that stage, things become complicated, however.

Some handset manufacturers may want to get involved in pixel-level processing. But de Luca warns that there is more experience than might be apparent involved in such seemingly simple issues as white balance. "There are lots of algorithms out there that will do a good job in a studio setting if you aim a lamp right at a subject," de Luca says. "But how realistic a use scenario is that? It takes a lot more sophistication to deal with a real-world scene that has a large dynamic range and several types of illumination. There's a lot of IP that belongs to companies in the photographic business."

The ownership of such IP may help determine partitioning by default. If an OEM selects one vendor's sensor and wants to use another vendor's image-processing algorithms, the result may of necessity be a multidie module.

LEGACY ISSUES

Another important influence on partitioning decisions is the legacy of the design team. "In the end, there are many algorithms available for each function," observes Toshiba's Burt. "Sometimes, companies just get wedded to one particular approach; they show almost a religious reluctance to change."

Such conservatism may come from simple inertia, or it may come from more political issues. If an OEM has chosen a powerful—and costly—application processor, for example, it may become an unspoken design requirement to find tasks that justify the processor's existence. This requirement may lead to skewed pipelines. In the Apple iPhone, for example, Apple reportedly demanded that there be no ISP. Instead, raw pixels pass directly to the graphics or application processor for pixel-level operations. This choice can save on hardware, but the loss of a dedicated signal processor in the pipeline can mean additional delays after the user presses the shutter button, as the general-purpose application processor scrambles to collect the statistics necessary to capture a full-resolution image.

A SEA CHANGE

Today, integration, IP selection, and culture help determine pipeline partitioning. But a new concept in camera-module design could alter many of the principles this article discusses. This concept—EDOF (extended depth of focus)—requires optimization across the entire camera module. The principle is less than obvious to designers unfamiliar with physical optics (see **sidebar** "A brief explanation of EDOF"). In short and contrary to all your experience with cameras or eyes, EDOF allows virtually everything in front of the camera lens to be in focus at the same time. A demon-

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stration photo from Tessera—the packaging company that recently purchased EDOF start-up Eyesquad and has incorporated EDOF into its product offerings—shows a man holding a business card up to the camera. The business card, the man, and the distant background are all in focus.

With conventional optics, this scenario would have required an extremely small aperture—perhaps a pinhole. The image would suffer from lack of sharpness and the usual problems of low-light photography, all due to the small aperture. But with EDOF technology, you can create such images using a wide aperture. EDOF technology has the obvious advantage that it eliminates the need for electromechanical-focusing arrangements and for autofocus algorithms. It can also permit the use of larger apertures to keep those increasingly small pixels well-fed with photons. And it can in some cases relax mechanical tolerances. As theorists explore the algorithms, there may be other benefits, as well, such as software zoom that does not butcher image quality. Soft zoom is under investigation at Eyesquad, according to Tessera Director of Technical Strategy Christopher Aubuchon.

But EDOF technology will have another kind of impact. The concept requires coordinated modifications to the physical lens, to the pixel-level processing algorithms, and, in many cases, to the ISP hardware. Aubuchon explains that there are many approaches to EDOF implementation, trading off lens complexity for computational demands for image quality. It is possible to end up with a very demanding lens design, large computational requirements, or seriously compromised image SNR (signal-to-noise ratio). It is also possible to find a local optimum that matches the needs of a particular OEM.

"There is not much motivation for a high-end DSC or even high-end-handset manufacturer to eliminate mechanical focus," admits Tessera's vice president of corporate development, John Keating. "But in the midrange—feature phones, for example—where image quality is important but a very small module is equally important—there is fertile ground for this technology. In the long run, I think you will see EDOF penetrate some of the DSC market, as well." Each of these markets may use a different lens design with a different image-reconstruction algorithm.

There has been a trend in the camera-module business for CMOS-imaging chips, optical assemblies, and algorithms to specialize so that sophisticated OEMs could mix and match, working with several partners to create an integrated module. But the value—and the impenetrability—of EDOF technology may reverse this trend, forcing OEMs to put their fate into the hands of an EDOF-capable vendor that can work magic on the optical path, ISP, and software all at once. This scenario could give a few start-up companies, such as dBlur, and quick-to-act larger companies, such as Tessera, an outsized influence in the OEMs' partitioning decisions, in effect giving these IP vendors system-integration authority. And that outcome would make the OEM not the final arbiter but merely another interested party in imaging-system-partitioning decisions.EDN

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TAKING A BITE OUT OF POWER:

TECHNIQUES FOR LOW-POWER-ASIC DESIGN

BY MICHAEL SANTARINI • SENIOR EDITOR

EVEN IF YOU ARE DESIGNING AN ASIC OR SOC THAT DOESN'T TARGET A LOW-POWER APPLICATION, YOU NEED TO BECOME FAMILIAR WITH LOW-POWER-DESIGN TECHNIQUES, BECAUSE THE NEWEST GENERATION OF SILICON-PROCESS TECHNOLOGIES INHERENTLY LEAKS POWER.

Until recently, low-power-digital-IC design has been an area for specialist or guru IC designers. However, most IC-design engineers will have to learn a variety of low-power-design techniques as ASICs and SOCs (systems on chips) increasingly target processes of 130 nm and below. At 130-nm processes, foundries started to employ new techniques and materials, such as low-k dielectrics and copper, in silicon processes to increase design performance. However, smaller geometries, scaled thresholds, and unscaled voltages produced smaller, speedier ICs but produced a nasty side effect: leakage, or static power. By the 90-nm node, power management started to become a huge concern, and, at the 65-nm node, low-power-design techniques are a must.

"As we scale technology nodes, clearly we have to lower V_{DD} [supply voltage], because there is a quadratic relationship: The power dissipation is proportional to V_{DD}^2," says Mike Keating, a fellow at Synopsys. "If we just scaled the devices and did not scale V_{DD}, we'd be doubling the power density every generation. We can't do that, so we've been lowering V_{DD}."

When the semiconductor industry lowered supply voltage over the last few nodes, each reduction also lowered the transistor threshold voltage, which keeps drain-to-source current at a level that allows ICs to charge their output capacitors and thus increase the performance of ICs in those nodes. However, as the industry further decreased threshold voltage at each node, it forced the subthreshold leakage to also increase at each node. "As we've been shrinking processes, the gate-oxide thickness is so skinny now, gate leakage is increasing exponentially," says Keating. "Somewhere around 65 and 45 nm, you end up with dynamic power equal to subthreshold current and equal to the gate-leakage current. We have a train wreck; only, in this case, we have three trains—dynamic power, subthreshold leakage, and gate leakage—headed to exactly the same spot."

AT A GLANCE

- At the 45-nm node, leakage power consumes 60% of an IC's total power.
- Foundries now offer several libraries, each with multiple threshold voltages to manage power.
- The EDA industry has split in its support of two similar power standards: UPF (Unified Power Format) and CPF (Common Power Format).
- Clock gating is one of the oldest tricks in the book, but power gating is quickly becoming the hottest technique for low-power design.

In the past, overall power density has essentially stayed the same for every process reduction. But, in 2005, the ITRS (International Technology Roadmap for Semiconductors) released a study that indicated that at the 65-nm node, dynamic-power density and leakage power would increase by 1.43 and 2.5 times, respectively. At the 45-nm node, the ITRS predicts, dynamic-power and leakage-power density will increase to two and 6.5 times, respectively. In reality, designs in high-speed 65-nm processes lose as much as half their power to leakage. Many in the industry believe that, by the 45-nm node, ICs will lose as much as 60% of their power to leakage (**Figure 1**). "Until recently, we've been dealing with power by simply making different trade-offs in silicon," says Keating. "That option is sort of disappearing. Using these design techniques is no longer an option; it is a requirement."

To deal with power management, the electronics community is employing new low-power techniques and materials on several fronts (**Figure 2**). Fabs have introduced multithreshold, multivoltage transistors; SOI (silicon-on-insulator) and low-k materials; body, or "back, biasing; and copper-metal and SiGe (silicon-germanium) substrates. Meanwhile, chip architects and software designers deal with low power by performing smart-hardware-versus-software trade-offs; by implementing power-savvy operating systems, introducing more hibernation modes into system design; and by more selectively granting memory access. IC designers are also employing several techniques to lower the power of their designs. The most popular techniques for low-power design include multithreshold design, multivoltage design, clock gating, power-aware memories, and power gating.

Jerry Frenkil, chief technology officer, vice president, and general manager of Sequence Design's Silicon Business Unit, notes that low-power design is all about reducing one or several parts of the power equation: Dynamic power plus leakage power equals the device's overall power consumption. Dynamic power is the power a device consumes when a user is employing it for its intended purpose, and leakage power is the power that leaking transistors waste (**Figure 3**).

Custom and circuit designers over the years have employed several techniques to lower the power of their designs, according to Kurt Keutzer, a professor at the University of California—Berkeley, who is a co-author and editor of *Closing the Power Gap Between ASIC & Custom: Tools and Techniques for Low Power Design* (**Reference 1**), which is due out by the time the Design Automation Con-

EDA INDUSTRY QUIBBLES OVER POWER STANDARDS

The EDA industry is responding to the challenges that designers face with power consumption. However, overcoming the low-power hurdle in a timely manner will likely require EDA vendors to collaborate on a common power format. Unfortunately, on the power front, the industry splits into two camps: A few small EDA companies back Cadence's CPF (Common Power Format), under the auspices of Si2 (Silicon Integration Initiative, www.si2.org), whereas Synopsys, Mentor, and Magma back Accellera's (www.accellera.org) UPF (Unified Power Format). Recently, it looked as if the two formats would merge under the IEEE, but politics in the industry have at least momentarily dashed the hope of that development. Ironically, those who have had access to both formats say that UPF and CPF share roughly 85% of the same functions. However, the EDA companies are guarding their formats in the hope that they will become de facto standards and thus be able to capture market share in a new tool area.

For now, it looks as though users and EDA vendors will have to support two formats. The industry and the designers have done it before with Verilog and VHDL–both viable HDLs (hardware-description languages). However, working with and supporting two formats create confusion, mistakes, delays, and more work for designers and vendors alike. One vendor notes that supporting two formats means that his company must allocate engineers to ensure that its tools support both formats. That requirement gives engineers less time to create tools to address tomorrow's challenges.

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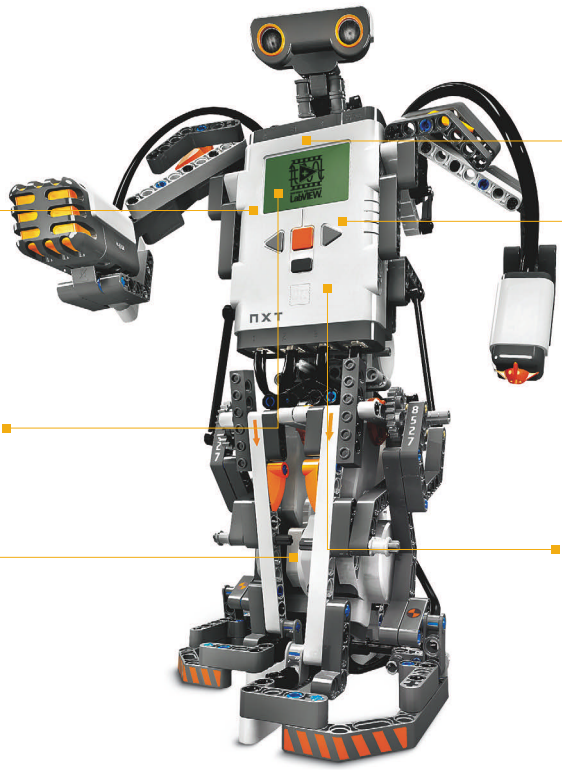

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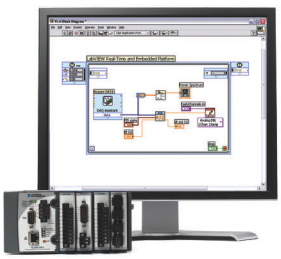

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ference takes place this June. However, he says, the power consumption of today's typical ASICs may be three to seven times that of custom ICs fabricated in process technology of the same generation. He and one of the book's co-authors, David Chinnery, estimate that, by employing low-power-design techniques, users can improve energy efficiency of their ASIC designs by a factor of two to three. "The main finding is that ASIC designers are leaving a lot of power savings on the table," says Keutzer.

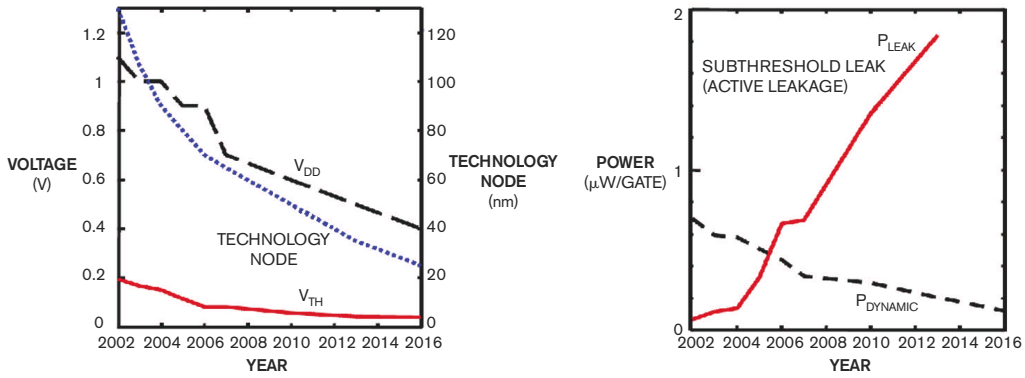

Figure 1 As vendors introduce processes with faster transistors and lower supply voltages, power leakage increases exponentially.

But there's no silver bullet in low-power design. "There are a lot of techniques … and different methods attack different portions of the power equation. They usually have some overhead of some sort," says Frenkil, also a contributor to the book. "Some may have no overhead, others may affect you in area, and others may affect you in speed. One of the critical things about low-power design is understanding the impact of what you are facing and how you are going to deal with it." Indeed, users will have to mix and match many of these techniques to come up with a low-power methodology that works for them.

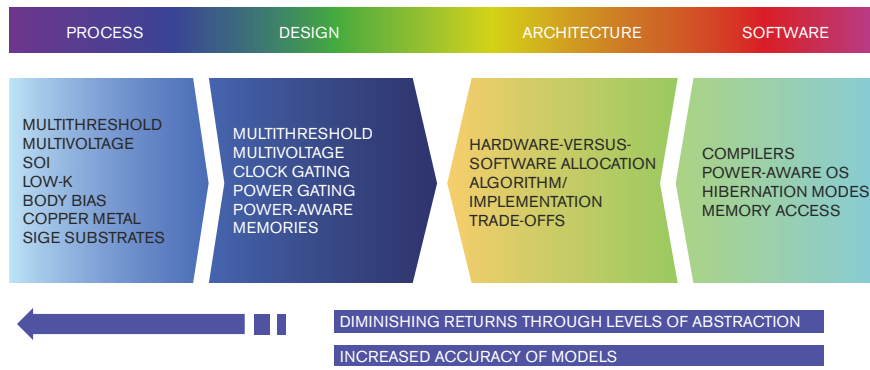

Figure 2 The industry is attacking power on several fronts. Foundries, IC-architecture design, software, IC design, and EDA are all pitching in to reduce power.

MULTITHRESHOLD DESIGN

About five years ago, when excessive power consumption became a problem, foundries started to offer libraries for low-power and high-speed design. For example, TSMC (Taiwan Semiconductor Manufacturing Co, www.tsmc.com) offers a standard, or nominal, library; a high-speed library; and a low-power library, each having several types of cells. For instance, each of TSMC's libraries includes low-threshold-voltage, high-threshold-voltage, and threshold-voltage-with-MTCMOS (multithreshold-CMOS) cells. Multiple-cell libraries help designers deal with both leakage and dynamic power. To deal with leakage power using multiple types of cells, designers today employ multithreshold design. "Because we've played so many games with V_{DD} and V_{TH} [threshold voltage], we can't create one library that is going to work for an entire design, because you have designs that are speed-critical, and, for the areas that are not speed-critical, you want to reduce the leakage," says Keating.

A multicell library typically comprises at least two sets of identical cells that have different threshold voltages. Those with higher threshold voltage are slower but have less leakage; conversely, the cells with lower threshold voltage are faster but leak. "It is a nonlinear relationship," says Keating. "Conceding a little bit of speed, you get a very dramatic reduction in leakage." Frenkil says that a high-threshold-voltage cell typically has 50% less leakage than a low-threshold-voltage cell with no bad side effects, such as area gain.

For most applications, designers typically use a low-threshold-voltage library for a first pass through synthesis to get maximum performance and meet timing goals. They then determine the critical paths in their design—that is, the path or paths in the design that require the highest performance. They then try to locate areas that don't require low-threshold-voltage cells and swap out low-voltage cells for high-voltage cells to reduce overall power and leakage of the design. Frenkil notes that this approach represents the most common use of the multithreshold-design technique because most applications have timing as a first requirement, low-threshold-voltage libraries run faster through synthesis, and synthesis tools ultimately produce smaller design areas from these libraries. Synthesis tools tend to run longer and produce larger design areas when running heavy doses of high-threshold-voltage cells.

However, in some wireless-system applications, power is the main goal, and area increases are less of an issue. In those cases, some designers first run synthesis with high-threshold-voltage cells, find the critical path, and then swap out the

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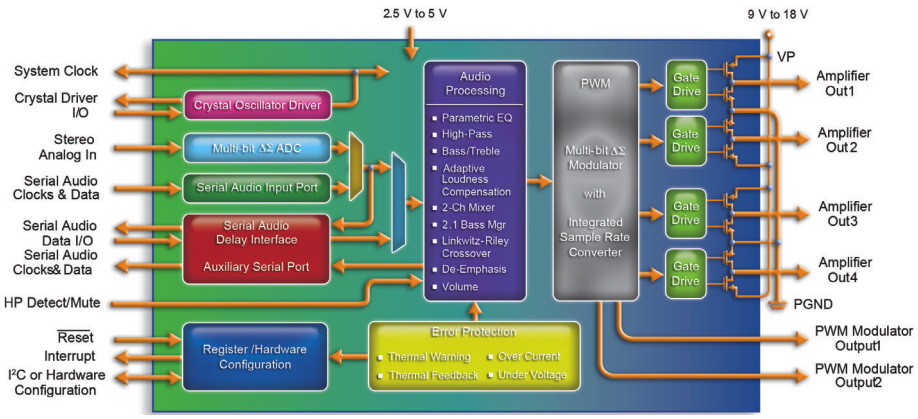

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CS44130	60 W	107 dB	0.12%	4	VP = 10.8 V to 21 V; VD = 3.3 V or 5 V; VL = 2.5 V to 5 V	Quad Power Stage IC Thermally Enhanced 90% Efficiency	48 QFN
CS44600	N/A	100 dB	<0.05%	6	VD = 2.5 V; VL = 3.3 V to 5 V	192 kHz Digital Amplifier Controller	64 LQFP
CS44800	N/A	100 dB	<0.05%	8	VD = 2.5 V; VL = 3.3 V to 5 V	192 kHz Digital Amplifier Controller	64 LQFP

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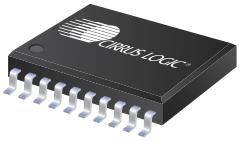

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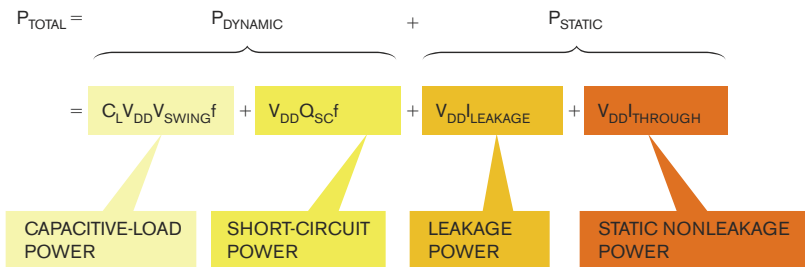


Figure 3 Low-power design is all about reducing dynamic power or leakage power in the total-power equation.

high-voltage cells with low-voltage cells until they reach their performance goal.

MULTIVOLTAGE DESIGN

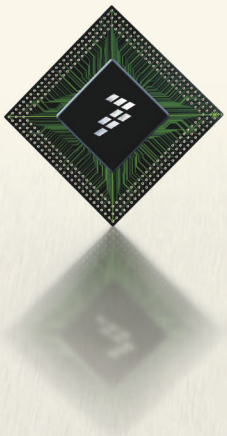
Although multithreshold design helps engineers minimize leakage of their designs through the use of multiple libraries, another technique, multivoltage design, helps designers control dynamic power. Similar to multithreshold design, multivoltage design enables designers to give the critical paths and blocks in their designs access to maximum voltage for the process and specification, but the designers then reduce the voltage for less power-hungry blocks. For example, Keating says, a processor block may require a clock speed of 500 MHz, but a USB core may require only 30 MHz to comply with the USB protocol and thus require less voltage to run. So, if designers give the USB core only the power it needs, they can drastically reduce the overall power the design consumes. To implement the method, designers traditionally put level shifters between blocks that are running at different voltages. "If you have a 0.9V region on your IC design that is sending a signal to a 1.2V region, you have to put a level shifter between the two regions so you can boost it to the swing in voltage and control timing," Keating says.

Although a fairly simple concept, its implementation is more complex. First, designers must get used to dealing with multiple voltages on a die. "We are really trained as engineers that a chip has just one power supply, and now you have to deal with some complications," says Keating. There are also some fairly significant challenges on the tools front. Most commercial synthesis and physical-design tools can insert level shifters and can perform multivoltage, but creating RTL is a problem. "HDLs don't yet have a mechanism for describing power connectivity," says Keating. This lack is one area that EDA vendors are addressing by trying to implement a low-power standard. Unfortunately, the industry players have diverged between two similar standards (see **sidebar** "EDA industry quibbles over power standards").

Another emerging method that started in custom design but is making its way into ASIC design is the use of parallelism along with voltage scaling. In their book, Chinnery and Keutzer describe this technique. Keutzer says that people at first dismissed it as impractical but that it is now getting serious attention. "You parallelize to get the performance up and then scale voltage down to reduce the power and energy," says Keutzer. "If you look at dynamic power, voltage is clearly where the biggest gains will be. So, how do you get the voltage down? Given a timing constraint—2 nsec, for example—you first overachieve your timing objective. In particular, you add parallelism to get the critical path down to 1.2 nsec. Then, you can scale down the voltage to relax back to the 2-nsec cycle time you need to achieve. The decrease in voltage more than compensates for the increase in area."

CLOCK GATING

Probably the oldest and most tried-and-true technique for reducing power is clock gating. One-third to one-half of an IC design's dynamic power is in the chip's clock-distribution system. "It's a pretty simple concept: If you don't need a clock running, shut it down," says Keating. Today, the two popular methods of clock gating are local and global (**Figure 4**). If you feed old data to the output of a flip-flop back into its input through a multiplexer, you typically need not clock again. Therefore, you can replace each feedback multiplexer with a clock-gating cell that clocks the signal off. You would then use the enable signal that



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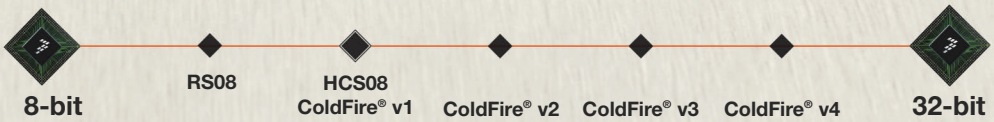

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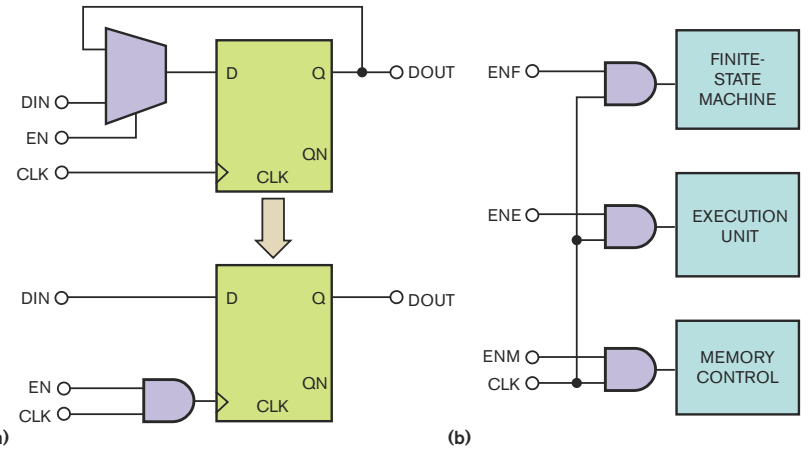

Figure 4 Local clock gating involves the use of an enable signal to gate the clock instead of multiplexing the data (a). Global clock gating reduces dynamic power by preventing the clock from transitioning when an enable is false (b).

controls the multiplexer to control the clock cell to clock the signal off.

In the old days of digital design, designers had to manually perform this task, but any commercial synthesis tool worth its salt can now automatically do it. "The tools are all set up for that now, so they will go in, automatically look for multiplexers, and, if there is a feedback multiplexer, they'll replace it with a clock-gating cell," says Keating. "When you start talking about 32-bit registers, you can get significant savings using this technique." He notes that Intel (www.intel.com) engineers this year presented a paper at SNUG (Synopsys Users Group) that reported a 43% savings in dynamic power using the technique (**Reference 2**).

The other popular approach of clock gating, global clock gating, is to simply turn off the clock to the whole block, typically from a central-clock-generator module. This method functionally shuts down the block, unlike local clock gating, but even further reduces dynamic power because it shuts down the entire clock tree.

POWER-SAVVY MEMORY

Another popular technique for lowering both dynamic power and leakage is to use power-aware memories.

In its simplest form, the technique involves shutting down segments of a memory array when they are not in use. Another technique in this category is body-biasing memories. In this method, designers reverse-bias a memory when it is not in use, which essentially raises the threshold voltage and in turn slows leakage. Another technique gaining popularity is to use multimode power for memories. In this technique, designers employ memory with several power modes. Many designs employ dual-function memories so that, when the CPU accesses a memory to read or write data to run a main application, the memory receives full access to power to perform the operation. However, when the memory is not required to read or write, designers can program the memory to power down to a level at which the memory gets only enough power to retain its memory content.

POWER GATING/MTCMOS

Perhaps the hottest new methods for low-power design are power gating and MTCMOS (**Figure 5**). Like voltage gating, power gating involves temporarily shutting down blocks in a design when the blocks are not in use. And, like voltage gating, the technique is complex. "The neat thing about the other techniques is that they are pretty much all transparent to the design engineer," says Keating. "When I'm writing my RTL, I don't have to think about multithreshold, multivoltage, clock gating, or power-aware memories because someone else downstream has to worry about it. But with power gating, I have to worry about it at the RTL. I have to design a power controller that is going to control what blocks I need to shut down and when, and I have to think about what voltage I'm going to [need to] run different blocks."

Traditionally, two methods for power gating are fine-grained and coarse-grained. In fine-grained power gating,

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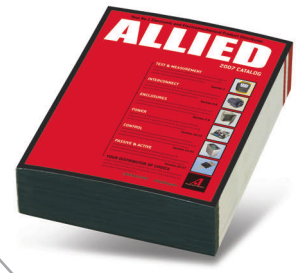

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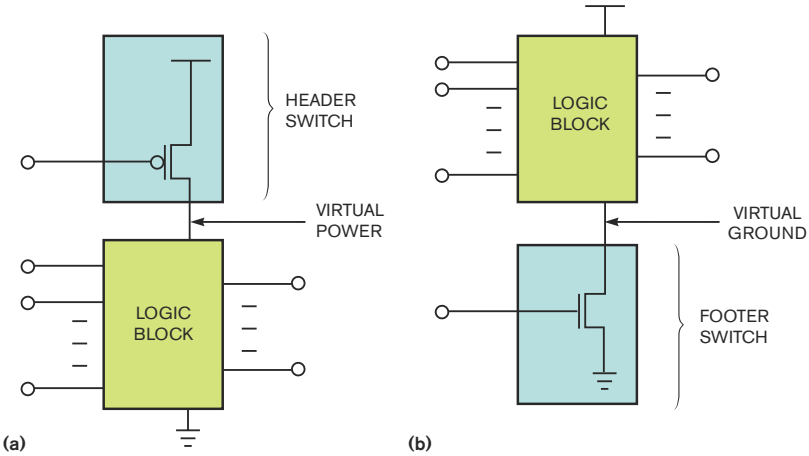

Figure 5 In MTCMOS and power gating, designers place a power-gating transistor in the stack between the logic transistors and either power or ground, thus creating a virtual supply rail (a) or a virtual ground rail (b).

designers place a switch transistor between ground and each gate. This approach allows designers to shut off the connection to ground whenever a series of functions is not in use. "You do that [technique] with every cell in the library," says Keating. "At first, people really liked fine-grained power gating because it is fairly easy to do power characterization of each cell, but the problem is the area hit is very significant: two to four times larger." Designers can also mix and match cells, having some power-gated and others not. Cells with high threshold voltage need not use power gating. For the most part, the power penalty is just too large, and many design groups are instead using coarse-grained power gating, in which designers create a power-switch network—essentially, a group of switch transistors that in parallel turn entire blocks on and off. The technique does not have the area hit of the fine-grained technique but is harder to characterize on a cell-by-cell basis.

Sequence Design's Frenkil says that a compromise—medium-grained power gating—is also starting to emerge in the design community. In this method, he says, "Power-gating cells will power small blocks individually. … If you look at a high-performance, 65-nm process, the leakage can easily be 40 to 50% of your total power design. If you are designing a high-performance chip, you have to deal with an enormous amount of leakage, so people have several separate power domains controlled individually. I've seen one modestly sized chip that has 20 power domains; if you scale that up to a leading-edge chip, it will have over 100 power domains." That number would be too hard to control with either a true fine-grained or a true coarse-grained technique. Of all the techniques, power gating has the most promise, says Frenkil. "It reduces leakage more, and it will scale well into the future, where things like back-biasing will not," he says.

EDA vendors are feverishly attempting to automate the power-gating technique. The warring low-power standards, UPF (Unified Power Format) and CPF (Common Power Format), both aim to help design teams more effectively implement power-gating methods. Keating notes, for example, that, in UPF design, engineers still must design the power controller in RTL, but several tools help with the insertion of the power mesh, isolation cells, and retention registers into a design. "Instead of doing it in RTL, you can do it in a UPF command language and specify a certain number of blocks to be isolated," says Keating. "In one line, you can do what it would take many lines of RTL to do. The tools are smart enough to take those commands and insert them at the appropriate levels. Some get inserted during synthesis; others get inserted during place and route."

The method requires either manual or tool-automated insertion of isolation-retention flip-flops. "When you shut down a block, and its outputs go to a block that is still powered up, you have to worry about those power-down nodes floating, and they can float to the threshold voltage and create unwant-

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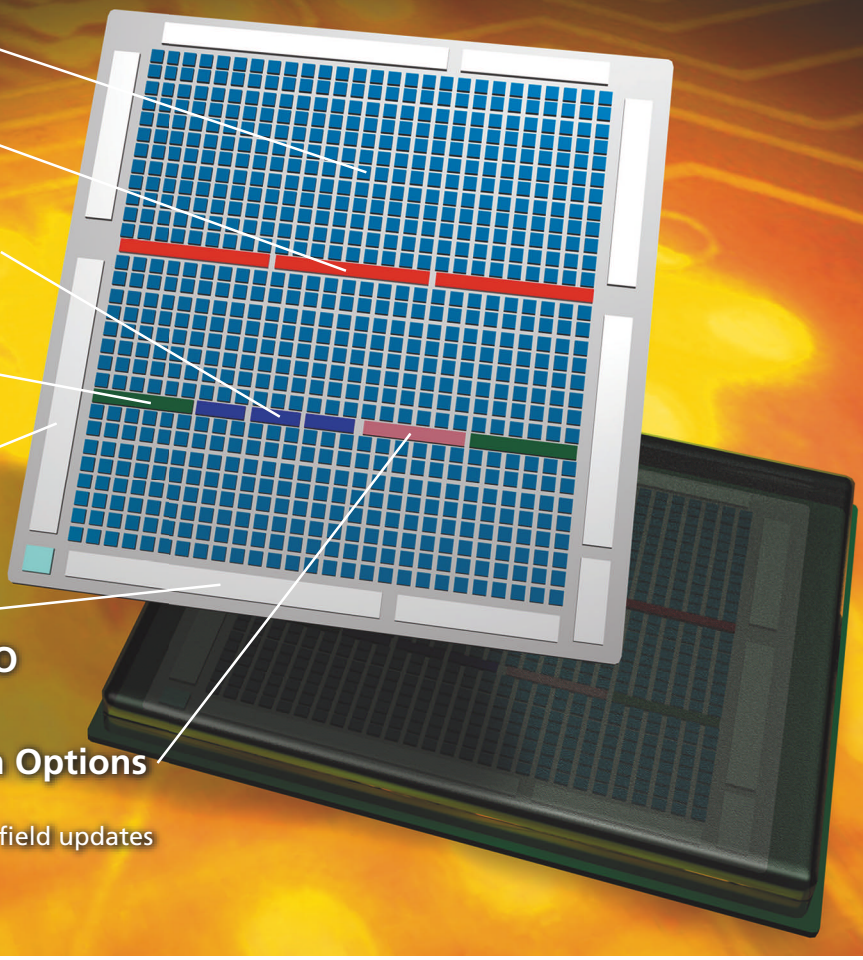

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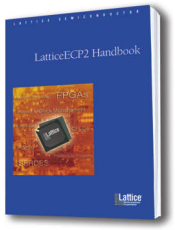

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ed currents downstream," says Keating. "You have to put isolation cells on those outputs and clamp that output to a one or a zero, so nothing gets hit by a floating current downstream."

The method also requires the use of retention flip-flops. Keating notes that one of the problems with shutting down a block is that the block needs to restore or maintain all its states. To achieve this goal, designers can use retention flip-flops, in which the main part of the flip-flop has a low threshold voltage—that is, fast but leaky—and it sits beside a balloon register of high-threshold-voltage, low-leakage cells. "Just before you shut down a block, you put the output of the flip-flop into a balloon register," says Keating. "Then, everything but the balloon register gets powered down to maintain the states. When the block powers back on, the balloon register dumps everything back on the main flip-flop, which helps quickly power the block up."

EDA TO THE RESCUE?

Frenkil notes that, although EDA vendors offer a wide range of tools to help designers implement low-power-design techniques, the EDA industry also offers power-integrity tools to help designers consider the effects of design decisions on power. Power-integrity tools perform voltage-drop analysis, voltage-derated timing analysis, noise-margin analysis, and power-bus sizing. Many vendors offer low-power tools to attack the problem from every angle (**Table 1** on pgs 60, 62, and 64). According to Keutzer, the EDA industry has yet to adequately address some problems. For example, the industry could provide tools that ease ASIC designers' ability to implement microarchitecture techniques, such as pipelining; to more efficiently lay out clock networks; and to more effectively use transparent latches. However, he notes, no EDA tool can solve everyone's power problem "It's not about home runs; rather, it's about a lot of singles," says Keutzer.

Designers must become familiar with a mix of low-power-design techniques and should also investigate which tools will help them achieve their power goals. The EDA industry is trying to market a healthy field of tools to help designers control power. Eventually, vendors hope to provide design flows to allow designers to make trade-offs among timing, power, signal integrity, and, eventually, even thermal analysis (**Reference 3**). Top semiconductor companies, design houses, and EDA players are trying to establish a common power format. Even with the current field of EDA tools and the rough beginnings of integrated low-power flows, however, the EDA industry still has much work to do before it can solve the power problem. EDN

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TABLE 1 LOW-POWER TOOLS

Company	Tool/ starting price	Tasks	Where used in flow?	Description
Apache Design	RedHawk-LP/ $95,000	Analysis	Postlayout (DEF/ GDS)	Low-power-design analysis and optimization tool, including rush-current and ramp-up analysis, full-chip mixed-mode verification, and switch optimization for MTCMOS designs
	RedHawk-ALP/ $150,000	Analysis	Postlayout (DEF/ GDS)	Extends RedHawk-LP to include ultralow-leakage-design techniques, such as substrate back-biasing (VTCMOS), power-gated memories, and on-chip low-dropout voltage regulators
ArchPro Design Automation	MVSim/ NA	Analysis and verification	RTL, gate level	Cosimulator that simulates multivoltage effects with electrical accuracy; users can identify multivoltage issues using automatic assertion generation and analyze coverage of multivoltage states
	MVRC/ NA	Analysis and verification	RTL, gate level	Vectorless verification of multivoltage issues; users can detect topological, functional, and sequential issues with respect to power-management control
	MVSyn/ NA	Design	RTL, gate level	Automatic insertion of level shifters and isolation cells at RTL and gate level; users can perform electrically accurate simulations at the RTL/gate level with the inserted cells
Atrenta	Spyglass-Power/ $60,000	Analysis	RTL, postsynthesis, after place and route	Provides a comprehensive approach to low-power design; helps manage power and voltage domains
Azuro	PowerCentric/ NA	Design and analysis	Gate level, postphysical	Operates as a complete replacement for clock-tree synthesis within digital-design flows, comprehensively addressing power, timing, and variability within one unified optimization environment
Bluespec	ESEComp/ $25,000	Design	ESL, RTL	Synthesizes SystemC designs into highly efficient Verilog RTL; enables rapid architectural exploration; accelerates the correct implementation of multiple clock domains, clock synchronizers, and gated clocks
	BSC/ $25,000	Design	ESL, RTL	Synthesizes Bluespec SystemVerilog designs into highly efficient Verilog Design; Bluespec's synthesis tools enable rapid architectural exploration and accelerate the correct implementation of multiple clock domains, clock synchronizers, and gated clocks
Cadence Design Systems	Cadence Low-Power Solution/ NA	Design and analysis	RTL, gate level, transistor level	Integrates logic-design, verification, and implementation technologies with the Si2 CPF; reduces risk; improves productivity; achieves superior trade-off among timing, power, and area requirements
	Encounter RTL Compiler global synthesis/ NA	Design and analysis	RTL, gate level	Performs top-down multiobjective, multidomain, multimode synthesis for exploration and synthesis of multiple threshold voltages, multiple supplies, power shutoff, and voltage scaling, using CPF to sustain design intent
	Encounter Conformal Low Power/ NA	Analysis	RTL, gate level, transistor level	Verifies and debugs power-optimized multimillion-gate designs using CPF and combining low-power structural and functional checks with equivalence checking for superior performance, capacity, and ease of use
	Encounter Test/ NA	Design	Gate level	Creates test mode for each power domain, including shutoff requirements, as specified in CPF; inserts structures to control power during test; generates ATPG vectors that reduce power consumption during test

Table continues on page 62

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Company	Tool/ starting price	Tasks	Where used in flow?	Description
	SoC Encounter/ NA	Design and analysis	Gate-to-GDSII	Implements low-power designs; includes multiple-power-domain support for virtual prototyping, placement, and optimization; provides autoinsertion of low-power structures, such as switch cells and isolation cells; includes power-aware clock-tree synthesis, domain-aware routing, analysis of power consumption and IR-drop effects
	Voltagestorm/ NA	Analysis	Gate level	Integrates static- and dynamic-power-rail verification in CPF-enabled SoC Encounter; performs sign-off power analysis; automates analysis and optimization of decoupling capacitance size and location, resulting in lower dynamic-IR drop
	Incisive Design Team and Enterprise Manager/ NA	Verification	System level, RTL, gate level	Creates power plan and metrics in CPF-enabled flow; tracks power verification metrics against design and verification plan, ensuring full coverage-driven verification of all power-modes in the design
	Incisive Design Team and Enterprice Simulator/ NA	Verification	System level, RTL, gate level	Uses CPF for seamless verification of power shutoff without changing the verification environment; reduces risk of power-shutoff failure
	Incisive Formal Verifier/ NA	Verification	System level, RTL, gate level	Verifies power intent using standard assertion languages, complex power-control modules, and state and sequence relationships versus CPF specification; identifies corner cases without time-consuming simulation
	Paladium III/ NA	Verification	System level, RTL, gate level	Emulates system-level behavior, including both software and hardware, to quickly verify complex power-shutoff relationships
	Xtreme III/ NA	Verification	RTL, gate level	Reduces verification risk by seamlessly and rapidly verifying power shutoff without changing the RTL or verification environment
ChipVision Design Systems	Orinoco/ $150,000	Design and analysis	Above RTL (system level)	Optimizes for low power at the electronic-system level to gain significant reduction of energy consumption
Golden Gate Technology	PowerGold/ $250,000 per year list price	Power optimization	Postsynthesis physical design, gate level	Reduces power by 10 to 20% or more without impacting timing and complementing Cadence, Synopsys, or Magma flows
Magma Design Automation	Talus Power/ NA	Design	RTL-to-GDSII	Enables optimal power management throughout the flow with power-aware synthesis, physical optimization, power-aware CTS, automated multivoltage, multiple threshold voltage, and MTCMOS methodology, allowing designers to minimize power and ensure uniform power distribution
	Quartz Rail/ NA	Analysis	RTL-to-GDSII	Analyzes power-integrity sign-off for power, IR drop, and thermal effects with a built-in SPICE engine for accurate results
Mentor Graphics	Questa 6.3/ TBD	Analysis	RTL, gate level	Simulates power shutdown and power-up of power domains; provides voltage scaling to reduce power gating and retention behavior in designs
	0-In CDC/ TBD	Analysis	RTL	Uses clock gating to reduce dynamic-power consumption; ensures the design has no clock-domain-crossing issues
Sequence Design	PowerTheater/ $115,000	Design and analysis	RTL, gate level	Provides RTL power analysis and management with silicon-aware features for voltage islands, multiple threshold voltages, power gating, and clock gating

Table continues on page 64

Intersil USB Switches

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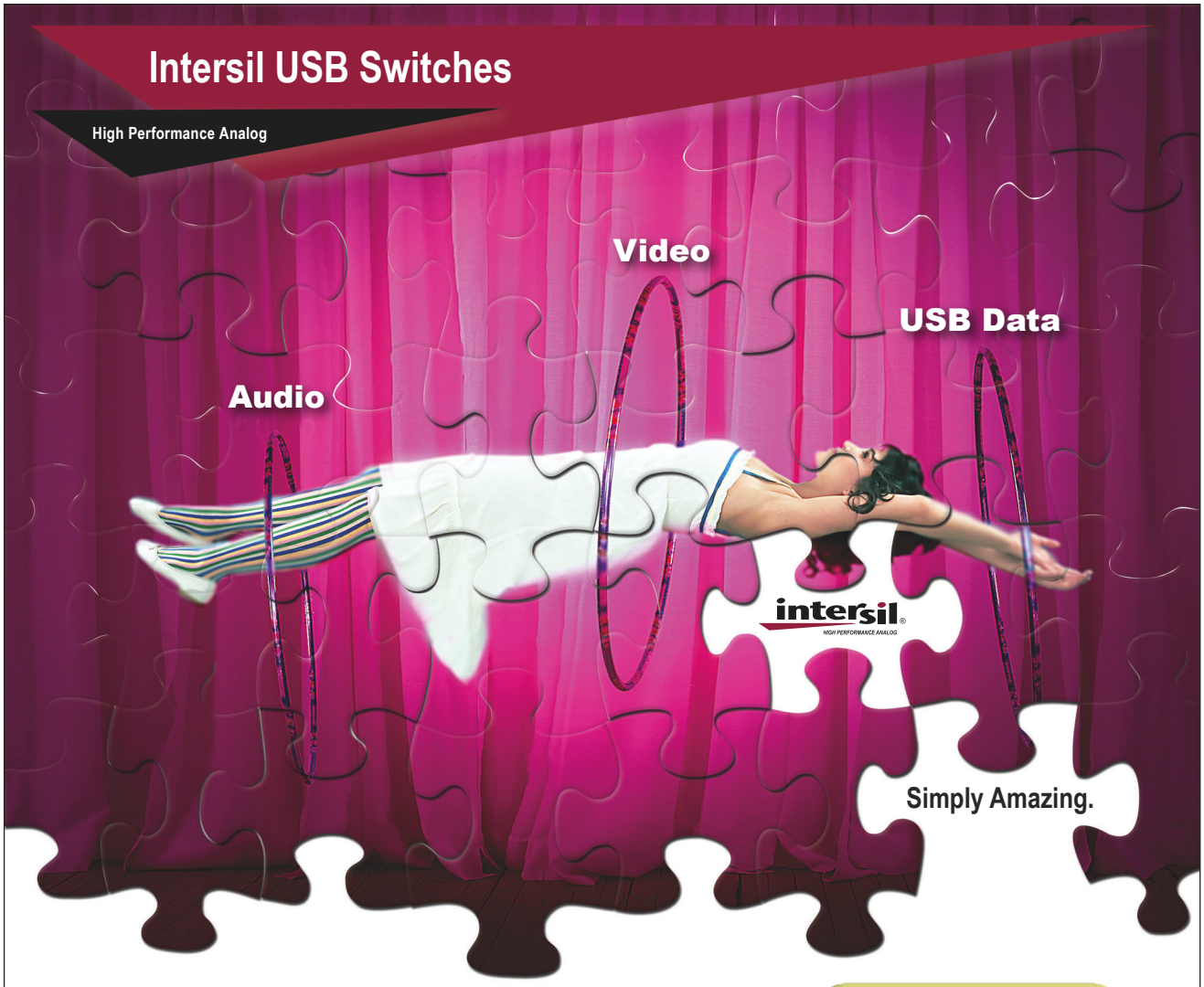

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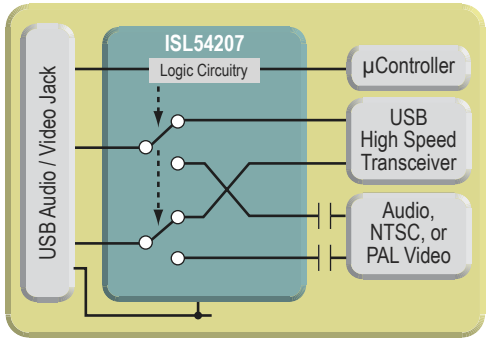

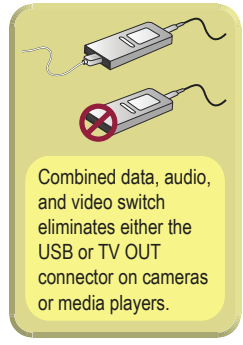

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Device	Audio THD 32Ω (%)	USB Speed	Video Diff Gain Phase
ISL54207	0.06	480	0.28 / 0.04
ISL54208	0.06	480	0.28 / 0.04
ISL54415	0.007	12	0.04 / 0.03
ISL54416	0.007	12	0.04 / 0.03
ISL54417	0.007	12	0.04 / 0.03

Audio / Data

Device	Audio THD 32Ω (%)	USB Speed
ISL54205A	0.06	480
ISL54206	0.06	480
ISL54400	0.007	12
ISL54401	0.007	12
ISL54402	0.007	12

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	CoolTime/ $130,000	Analysis	Physical design	Provides dynamic voltage-drop analysis and optimization; analyzes timing, signal integrity, static-IR drop, and electromigration; supports design techniques, such as voltage islands, multiple threshold voltages, power gating, and clock gating
	CoolCheck/ $80,000	Analysis	Physical design	Provides early power-grid debugging with a fast formal technique for finding missing vias, weak connections, and highly resistive current paths in the power grid
	CoolPower/ $240,000	Design and analysis	Postroute design closure	Provides automatic, concurrent optimization of leakage power, dynamic power, timing, and signal integrity, including multiple threshold voltages and MTCMOS power-gating optimizations
Synopsys	VCS/ $36,750	Verification	RTL, gate level	Provides comprehensive functional verification with built-in testbench, coverage, assertion, and debugging technology; supports power-aware verification, including correct handling of retention registers, and power-up/power-down sequences
	Leda/ $14,945	Analysis	RTL, gate level	Provides programmable RTL design and coding-guideline checker and built-in checks for CDC, SDC, power, and test; provides more than 50 low-power checks, including insertion/location of level shifers and isolation cells and clock gating to turn off power regions
	Design Compiler Ultra/ $98,000	Design	RTL	Provides comprehensive RTL synthesis, delivering best productivity; includes power and test-aware Topographical Technology
	Power Compiler (add-on to Design Compiler Ultra)/ $50,470	Design	RTL, gate level	Provides complete power-management synthesis for achieving the lowest power design; supports multivoltage, MTCMOS power gating, multithreshold leakage and gate-level power optimization, clock gating, and operand isolation
	DFT MAX (add-on to DFT Compiler)/ $123,725	Design	Gate level	Provides power-aware adaptive-scan compression for test data and time reduction
	IC Compiler/ $757,050	Design and analysis	Gate level	Provides complete physical implementation, including hierarchical-design planning with automated power-network synthesis and analysis; provides single convergent flow from netlist to silicon with support for multivoltage designs, multithreshold leakage, low-power placement and CTS, and state-retention power gating
	PrimeTime PX/ $24,500	Analysis	Gate level, TTL	Provides concurrent timing, signal integrity, and power analysis
	PrimeRail/ $176,645	Analysis	Gate level, TTL	Offers power-integrity sign-off with full-chip dynamic-power-integrity tool; provides cell- and transistor-level dynamic-voltage-drop and electromigration analysis
	TetraMAX/ $54,145	Analysis	Gate level	Offers power-aware manufacturing-test-pattern generation for designs incorporating scan design-for-test techniques, including compression
	Innovator/ $60,000	Preimplementation	Transaction (system) level	Provides software-driven power analysis and optimization with power-aware system software to measure the effects of architecture, power-management techniques, and software on power dissipation

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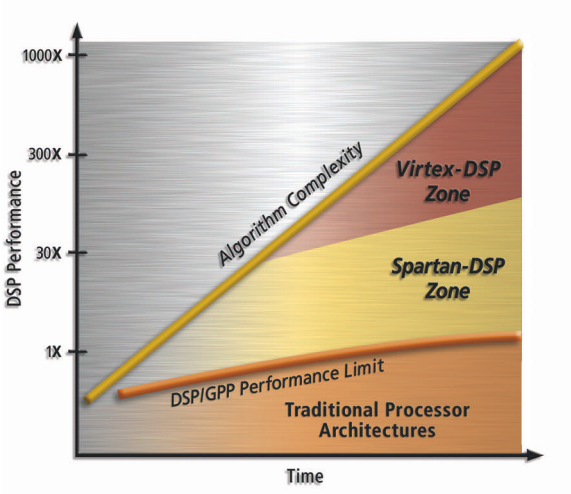

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ANALOG-TO-DIGITAL CONVERTER ICs

Volume 7, Issue 3

YOUR SEMICONDUCTOR SOLUTIONS RESOURCE

FEATURED ARTICLES

At 5 MSPS and 35 mW Power, this 12-Bit SAR ADC Makes Choosing ADI Easy

Motor control and automotive customers need high speed, zero latency, simultaneous sampling ADCs to achieve the highest efficiency and precision control, while consuming a minimum of power. Meeting these demands in a compact footprint is a challenge faced by all IC suppliers.

Solution

The AD7356 12-bit, 5 MSPS, dual-channel simultaneous sampling ADC is unlike any other SAR that ADI offers. It is 25% faster than other single channel SAR ADCs in the 12-bit resolution range and three times faster than the next fastest simultaneous sampling SAR ADC.

The higher data throughput rate offered by the AD7356, with no limitation on time between conversions, provides a key performance advantage for devices such as optical encoders used in high speed industrial motor controls where continuous measurement of motor functions is required to maintain precision operation.

The AD7356 is also suitable for adaptive cruise control and RFID automotive applications. It provides complete functionality for fast I & Q sampling, consumes just 35 mW of power, and is available in a compact 16-lead TSSOP package. The AD7356 conversion process and data acquisition use standard control inputs to allow for easy interfacing to DSPs. For optimum performance, the AD8138 ADC driver, which offers low distortion and fast settling times, is recommended. Other leading ADI SAR ADCs are shown in the table below.

- Simultaneous sampling ADC
- Resolution: 12-bits
- Throughput: 5 MSPS per channel
- Low power: 35 mW at 5 MSPS
- On-chip reference
- Zero latency
- Package: small 16-lead TSSOP

AD7356

APPLICATIONS
- Industrial motion control
- Adaptive cruise control (ACC)
- RFID transceivers

$7.89

Part Number	Description (SAR ADC)	Maximum Power (mW)	Package	Price ($U.S.)
AD7356	Dual, 5 MSPS, 12-bit, 1-channel	35	16-lead TSSOP	7.89
AD7266	Dual, 2 MSPS, 12-bit, 3-channel	27	32-lead LFCSP, 32-lead TQFP	7.55
AD7265	Dual, 1 MSPS, 12-bit, 3-channel	7	32-lead LFCSP, 32-lead TQFP	5.75
AD7866	Dual, 1 MSPS, 12-bit, 2-channel	11.4	20-lead TSSOP	5.95

All prices in this bulletin are in USD in quantities greater than 1000 (unless otherwise noted), recommended lowest grade resale, FOB U.S.A.

Dual, 150 MSPS ADC Simplifies Infrastructure Design

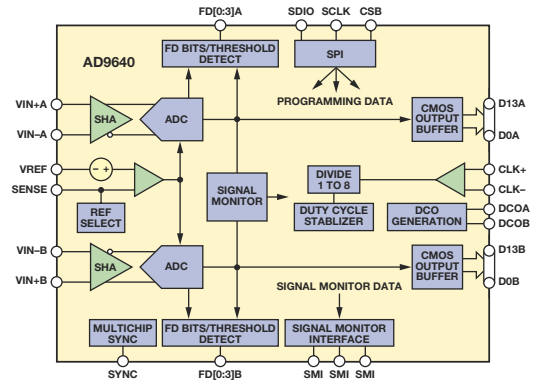
As usage and demand for competitive cell phone services continue to rise, wireless infrastructure manufacturers must constantly reduce the size and cost of newly installed wireless infrastructure, while holding to the highest standards of performance, functionality, and quality of service. The data conversion block is a critical function in wireless infrastructure designs, and selecting the best converter is key to improving the overall system design by breaking through design barriers such as performance, size, and cost.

Solution

In the main receiver function, the ADC is the key block that digitizes the incoming intermediate frequency (IF) signal after it has been mixed down from the antenna. It then passes the digital data to the digital downconverter. Currently, most architectures require two receivers, each requiring a high performance, high speed ADC. Sampling rates beyond 135 MSPS could only be realized via single-channel 14-bit ADCs—requiring two separate converter blocks, thus driving increased power consumption, PCB area, and cost.

ADI's new dual, 14-bit, 150 MSPS AD9640 ADC enables a 50% reduction in converter board space in the main and diversity architecture. With a relatively low 390 mW/channel power consumption, the AD9640 simplifies the mechanical and passive thermal design requirements of pole-mounted transceiver enclosures. The AD9640 is available in a 9 mm × 9 mm, 64-lead LFCSP.

AD9640: DUAL, 14-BIT, 150 MSPS ADC



APPLICATIONS

- Multimode digital receivers: GSM, EDGE, PHS, UMTS, W-CDMA, CDMA-ONE, IS95, CDMA2000, IMT-2000
- WiMAX
- Smart antenna systems
- General-purpose software radio

AD9640-150 $87.50

- SNR of 72.7 dBFS with 70 MHz A_{IN}
- SFDR of 85 dBc with 70 MHz A_{IN}
- IF sampling to 450 MHz

Online Seminar Series

"New Dimensions in Driving ADCs" at *www.analog.com/onlineseminars*.

Get the Most Performance from Your ADCs with Drivers that Won't Limit System Performance

The ADA4937-1 and ADA4938-1 set new performance standards (14-bits at 70 MHz and 16-bits at 40 MHz) in noise and distortion for differential ADC drivers. The devices enable design engineers to easily get the most performance out of their ADCs since amplifier distortion will not limit system performance. The adjustable level of the output common mode allows the ADA4937-1 and ADA4938-1 to match the input of the ADC.

ADA4937-1 Features

- –120 dBc/–102 dBc HD2/HD3 @ 10 MHz
- –98 dBc/–100 dBc HD2/HD3 @ 40 MHz
- –84 dBc/–90 dBc HD2/HD3 @ 70 MHz
- –3 dB BW @ 1.6 GHz, G = 1
- Slew rate: 5000 V/μs
- V_S = 3.3 V to 5 V

ADA4938-1 Features

- –112 dBc/–108 dBc HD2/HD3 @ 10 MHz
- –96 dBc/–93 dBc HD2/HD3 @ 30 MHz
- –79 dBc/–81 dBc HD2/HD3 @ 50 MHz
- –3 dB BW @ 1.5 GHz, G = 1
- Slew rate: 4700 V/μs
- V_S = 5 V to 10 V

ADA4937-1 and ADA4938-1 Common Features

- Input voltage noise: 2.2 nV/√Hz
- 0.1 dB gain flatness to 125 MHz
- Fast overdrive recovery to 4 ns
- 3 mm × 3 mm LFCSP
- Priced at $3.79

24-Bit, 128 kSPS ADC for Low Power Equipment

In applications such as data acquisition, vibration analysis, and instrumentation, where small or faint (low level) signals must be distinguished in the presence of larger signals, there is a need for low power, high precision analog-to-digital converters with excellent dc and ac specifications. To date, finding an ADC that excels on all these levels has been a challenge for designers.

Solution

Specifically designed for ultralow power data acquisition, the AD7766 provides 24-bit resolution with 16-bit INL performance and 108 dB SNR. The power dissipation is low—just 20 mW of power at a data rate of 128 kSPS, scaled throughout. Thus, the device is ideal for measuring small signal changes over a wide dynamic range. This requirement is particularly important in vibration analysis where small signal changes are measured on larger ac or dc signals—enabling early failure detection and improving overall equipment reliability. The AD7766 provides excellent dc accuracy and offset drift of just ±50 nV/°C, making it suitable where dc data also needs to be acquired. In sonar equipment, for example, the AD7766 best-in-class SNR, as high as 114 dB at a 32 kHz output data rate, enables feature identification at greater distances than previously possible. The AD7766 is available in a 16-lead TSSOP package.

Functions	Requirements	Typical Applications
Measuring a small ac on a larger dc bias	• Dynamic range/SNR • Need for dc specs	• General high quality 24-bit data acquistion • Vibration analysis • Bearing monitoring
Continuous acquisition of an ac signal with a wide dynamic range	• Dynamic range/SNR • Need for dc specs	• Radio and HF radio • Sonar

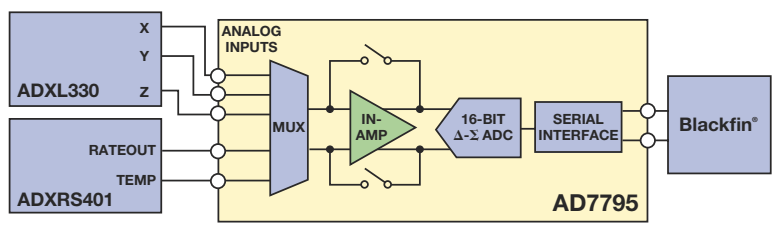
Σ-Δ ADCs Optimize Processing of MEMS Sensor Signals

Analog Devices offers a range of Σ-Δ ADCs for processing signals from MEMS accelerometers and gyros. When a car is in motion, GPS signals can be blocked by tall buildings and trees. In these cases, dead-reckoning is used to counter these negative phenomena. "Dead reckoning" is a method that utilizes accelerometers and gyros to measure the automobile speed and direction. ADI's extensive portfolio of these types of sensors includes the ADXL330 accelerometer and the ADXRS401 gyro.

The AD7795 is a 6-channel Σ-Δ ADC that can process the low frequency signals (typically around 100 Hz) of the gyro and the accelerometer 3-axis channels with 16-bit precision. With a low current consumption of less than 500 μA max, the AD7795 is particularly suited to consumer navigation units designed to detach from the automobile so that the device may be used by pedestrians as a portable navigation tool.

The AD7795 also includes an on-chip reference and oscillator—saving system board space and cost. The programmable gain function makes the AD7795 particularly useful for measuring low level temperature signals to compensate for sensor drift.

GPS NAVIGATION SIGNAL CHAIN



Part Number	Bits	Channels	Current (μA)	Gain	Update Rate (Hz)	Package	Price ($U.S.)
AD7795	16	6	450	1 to 128	4 to 470	24-lead TSSOP	4.40
AD7708	16	5, 10	1300	1 to 128	5 to 1300	28-lead SOIC	3.98
AD7794	24	6	450	1 to 128	4 to 470	24-lead TSSOP	5.80

For more information on Σ-Δ ADCs from ADI, visit *www.analog.com/sigma-delta*.

"Options and Solutions for Sensor Signal Conditioning" at *www.analog.com/onlineseminars*.

Online Seminar Series

For samples and data sheets, visit www.analog.com/V7ADC

ANALOG DEVICES

High Performance, Low Power, Small Package PulSAR® ADCs for Every Designer's Budget

In medical, industrial, instrumentation, and sensor equipment, low power consumption and portability are critical to performance optimization. Designers seek uncompromised performance, at reduced power, board space, and cost.

Solution

ADI's family of low power PulSAR ADCs in 10-lead MSOP and LFCSP packaging is ideal for challenging applications that require low power, extended battery life, and high channel integration. At any speed and resolution, at any price, our industry-leading portfolio of 14-bit, 16-bit, or 18-bit SAR ADCs in small packages makes it easy to select the best converter solution for your application. All ADCs within this family are pin-compatible—enabling flexible accommodation of system performance changes during system feasibility evaluations, leading to faster development times overall.

AD7982

The AD7982 is an 18-bit, 1 MSPS, PulSAR ADC, available in a 3 mm × 3 mm LFCSP, which is ideal for industrial and medical equipment such as CT scanners. It consumes just 7 mW power—95% less than the closest competing 18-bit ADC in its class, enabling longer battery life for portable equipment. It also has significant size advantage in the 10-lead LFCSP—80% smaller than any other 18-bit ADC capable of a 1 MSPS clock rate.

AD7980

The AD7980 is the industry's lowest power 16-bit SAR ADC—and consumes just 7 mW power, which scales linearly with the sampling rate. It operates from a single 2.5 V_{DD} power supply, and has a versatile serial interface port. The compact 3 mm × 3 mm LFCSP package represents a footprint reduction of over 80% vs. the competition. Many high speed data acquisition and automatic test equipment applications can take advantage of the outstanding dc and ac 16-bit performance. The wide dynamic range of the AD7980 allows low level signals to be converted with minimal front-end analog signal conditioning.

The ADA4941 and the ADA4841-x family of op amps are ideal to drive the PulSAR ADCs, and the ADR431 is a recommended supporting voltage reference.

For more information on PulSAR technology, visit *www.analog.com/PulSAR*.

APPLICATIONS

- High speed data acquisition
- Instrumentation
- Smart sensors
- Portable medical

Online Seminar Series

For "Simulating and Modeling A/D Converters to Simplify System Design," visit *www.analog.com/onlineseminars*.

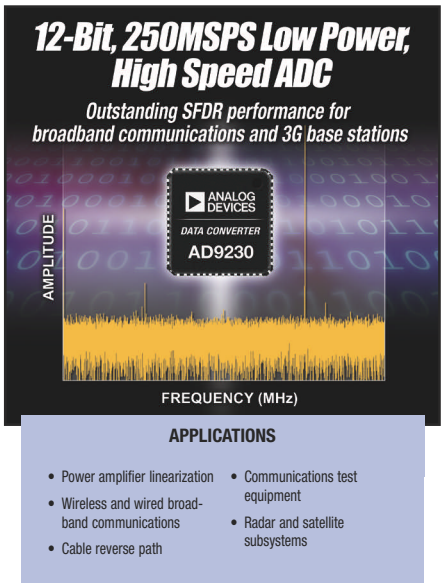
Part Number	Resolution (Bits)	Sample Rate	Maximum INL	SNR (dB)	Power @ 100 kSPS (Typ)	Package	Price ($U.S.)
AD7982	18	1 MSPS	±2 LSB (8 ppm)	99	700 µW	10-lead MSOP, 10-lead LFCSP	23.00
AD7690	18	400 kSPS	±1.5 LSB (6 ppm)	102	4.4 mW	10-lead MSOP, 10-lead LFCSP	19.50
AD7691	18	250 kSPS	±1.5 LSB (6 ppm)	102	1.4 (2.5 V)	10-lead MSOP, 10-lead LFCSP	14.50
AD7980	16	1 MSPS	±1.5 LSB (22 ppm)	91.5	700 µW	10-lead MSOP, 10-lead LFCSP	19.50
AD7693	16	500 kSPS	±0.5 LSB (7 ppm)	96.5	3.6 mW	10-lead MSOP, 10-lead LFCSP	18.00
AD7688	16	500 kSPS	±1.5 LSB (22 ppm)	95.5	3.75 mW	10-lead MSOP, 10-lead LFCSP	14.95
AD7685	16	250 kSPS	±2 LSB (30 ppm)	93.5	1.35 mW (2.5 V)	10-lead MSOP, 10-lead LFCSP	6.50
AD7683	16	100 kSPS	±3 LSB (45 ppm)	91	1.5 mW (2.7 V)	8-lead MSOP, 8-lead LFCSP	5.75
AD7942	14	250 kSPS	±1 LSB (60 ppm)	85	1.25 mW (2.5 V)	10-lead MSOP, 10-lead LFCSP	4.75

Lowering Power Consumption Threshold of ADCs for Wired and Wireless Communications

With the migration of 3G and 4G base station platforms that utilize digital predistortion techniques across various system form factors, such as picocells and microcells, total system power consumption becomes increasingly important due to system deployment constraints. Overall efficiency can be greatly improved by using predistortion feedback schemes that enable transmit operation near the power amplifier saturation point. Intermodulation products that interfere with adjacent channels can be "nulled" out by predistorting this signal. The digital feedback loop is used to measure the nonlinear behavior by means of digitizing a wide signal bandwidth and providing a correction signal that compensates for these transmit errors.

In broadband communication systems, such as cable modem termination systems (CMTS) and fixed point-to-point radios, a reduction in board area translates to higher channel counts or smaller end system form factors.

The AD9230/AD9211 families of 12-bit and 10-bit ADCs are specifically designed to support these system demands. This LVDS output-based family features the world's lowest ADC core power consumption performance at 400 mW while sampling at 250 MSPS in double data rate mode. The small, 56-lead, 8 mm × 8 mm LFCSP packaging allows system engineers to shrink total board area. In addition, these products offer superior dynamic performance of 64.9 dBFS signal-to-noise ratio (SNR) and 79 dBFS spurious-free dynamic range (SFDR) at 250 MSPS.



- 64.9 dBFS/59 dBFS SNR @ 70 MHz A_{IN}, 250 MSPS
- 79 dBc SFDR @ 70 MHz A_{IN}, 250 MSPS
- 1.8 V single supply
- AD9230 family: LVDS (DDR or SDR) outputs at 250 MSPS
- AD9626 family: CMOS full rate or demultiplexed outputs up to 250 MSPS
- 700 MHz full power analog bandwidth
- Clock duty cycle stabilizer
- Package: 36-lead LFCSP

Part Number	Resolution (MSPS)	Sampling Rate (Bits)	Power Dissipation (mW)	Price ($U.S.)
AD9230-250	12	250	400	59.00
AD9230-210	12	210	383	42.00
AD9230-170	12	170	350	35.00
AD9230-11-200	11	200	380	36.00
AD9211-300	10	250	400	46.00
AD9211-250	10	200	400	39.00
AD9211-200	10	170	385	32.00

"Options and Solutions for Frequency Synthesis" at *www.analog.com/onlineseminars*.

For "Using State of the Art in ADCs—The Dimensions of Performance in ADCs That Are Driving Markets," visit *www.analog.com/advancedADCs*.

Subpicosecond ADC Clock and Timing Solutions

ADI offers a portfolio of clock products that deliver low jitter, low phase noise, and low spurs—making them ideal for clocking high performance ADCs and DACs.

Our portfolio includes ultralow jitter clock distribution and clock generation products for wireless infrastructure, instrumentation, broadband, ATE, and other applications demanding subpicosecond performance. ADI clock ICs integrate PLL cores, VCOs, dividers, phase offset, skew adjust, and clock drivers in small chip scale packages.

Visit *www.analog.com/clocks*.

For samples and data sheets, visit www.analog.com/V7ADC

ANALOG DEVICES

New ADI Online Tool Enhances Simulation and Evaluation Capabilities for High Speed Data Converters

Many designers are familiar with ADIsimADC,™ a simulation tool that accurately models the typical performance of many of our high speed converters. Using ADIsimADC, a designer can simulate the performance of an ADC affected by different input frequencies, input amplitude, and clock jitter at ambient temperature. Our new tool, VisualAnalog,™ takes simulation to the next level by allowing the designer to create complex input signals for the ADC and to customize the analysis in order to refine the converter selection process.

Using a simple graphical user interface (GUI), the user can combine tone generators, Gaussian noise sources, customizable filter masks, and a pattern loader to evaluate an ADC with signals that are closer to real-world input signals. The user can also use quadrature data or merge two real waveforms into a complex interleaved waveform. These created waveforms can be utilized for the input to an ADC model or can be saved for later use with the digital pattern generator to be used for signal synthesis.

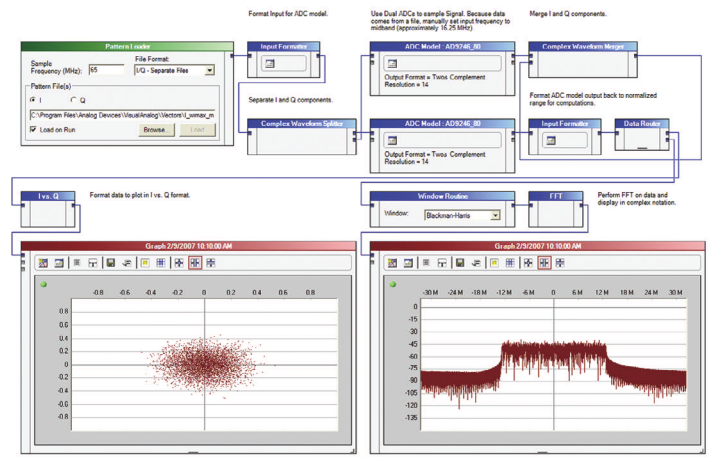
In addition to enabling the creation of complex waveforms, VisualAnalog includes additional data converter analysis previously unavailable from other tools. A designer can perform complex analysis showing I & Q constellation plots, track the peak of any value over many iterations, include or exclude specific spurs from noise calculations, as well as define a custom power calculation such as ACPR. This enhanced set of analysis functions applies to both the modeled ADC performance and data captured from an evaluation board.

With VisualAnalog, evaluation boards can also be configured whereby the software will automatically detect the ADC evaluation board in use (for ADCs that support SPI function) and preload those parameters to save time and effort. VisualAnalog also works with the DAC digital pattern generator to move data from a software data set to the hardware, thus allowing the user to generate specific waveforms when using a TxDAC® digital-to-analog converter evaluation platform.

After installing VisualAnalog software, the user can get started immediately by connecting an evaluation board and opening the default canvas for that selected product. Experienced users can open an existing template or create a custom template to solve any converter evaluation challenge. A complete user manual includes instructions and examples to help you start working with a blank canvas and create your own design. To download VisualAnalog, visit *www.analog.com/ADIsimADC*.

- Imports models from ADIsimADC online simulation tool
- Allows a user to create more complex input signals:
  - Tone generator for sine waves
  - Filter masks
  - Gaussian noise sources
  - Pattern loader
  - I & Q waveforms, including merging two real waveforms into a complex interleaved waveform
- Enables many types of complex analyses and calculations
- Autodetect data load function when used with ADI evaluation boards
- Compatible with DAC pattern generator interface (DPG interface)

VisualAnalog CONVERTER ANALYSIS PLATFORM



To view ADI's complete list of available online design tools, visit *www.analog.com/designcenter*.

Support components can make or break a successful converter implementation. View our online, on-demand technical seminar and learn from the experts. "Data Converter Support Components: Make the Right Choice!" is available at *www.analog.com/onlineseminars*.

Simplify Motion Control Designs with ADI's Flexible, Simultaneous Sampling ADCs

Measurement of a motor's position, speed, and load requires simultaneous sampling to achieve maximum accuracy in motor positioning. Analog Devices offers a wide range of precision analog-to-digital converters specifically designed to address this need. Shown below are examples of products that combine high resolution and speed, high voltage capability, flexibility, and high levels of integration that provide savings in both footprint and component count for the system designer.

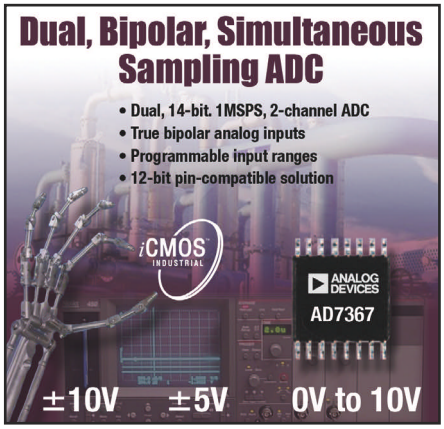
AD7264 is a 14-bit, 1 MSPS, dual, simultaneous sampling ADC. Each ADC is preceded by a true differential analog input with a PGA, providing gains of 1 to 128, enabling data acquisition boards to fit with a range of sensors, and reducing the signal conditioning typically associated with this function. The AD7264 features four integrated comparators, low power of 120 mW, is available in 48-lead TQFP, and is priced at $9.06. The AD7262 is a 12-bit, 1 MSPS, pin-compatible solution.

AD7367 is a 14-bit, 1 MSPS, dual, 2-channel, simultaneous sampling ADC that can accept true bipolar analog input signals in the ±10 V, ±5 V, and 0 V to 10 V ranges, is available in 24-lead TSSOP, and is priced at $7.55. The AD7366 is a 12-bit, 1 MSPS pin-compatible solution.

AD7656 is a highly integrated, 6-channel, 16-bit, 250 kSPS, simultaneous sampling *i*CMOS™ ADC offering the critical combination of speed, accuracy, and power required for design success in demanding industrial design applications. It is priced at $17.00. The AD8021 and AD8610 are recommended drivers to support the AD7656.

AD7328 is a true bipolar, 8-channel, low power, 13-bit resolution (12-bit plus sign), 1 MSPS *i*CMOS ADC. It can accommodate input voltage ranges up to ±10 V, and is available in 20-lead TSSOP. It is priced at $6.25.

For more information on these devices and other high performance SAR ADCs, visit *www.analog.com/ADCs* or *www.analog.com/motorcontrol*.



Multichannel, Low Power I²C® ADCs in Tiny SOT-23 Packaging

Multichannel I²C converters are ideal for monitoring miscellaneous voltages such as power supply or bias voltages that are outside the main signal chain yet are critical to system functionality and performance. Moreover, in an optimized design, this monitoring functionality needs to be achieved with minimal processor supervision.

Solution

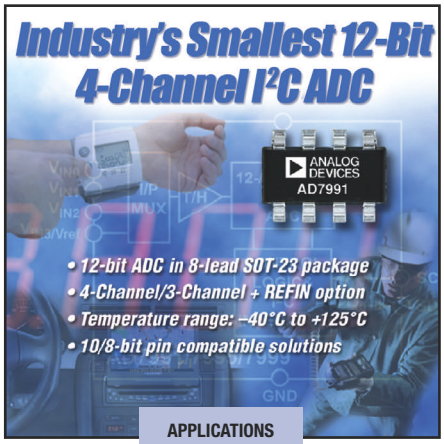
Analog Devices' multichannel I²C ADCs, the AD799x family, are unmatched in their ability to deliver the low power, small footprint, and low cost requirements that today's I²C system monitors demand. The AD7991 is the industry's smallest 4-channel, 12-bit ADC with I²C-compatible interface. The device normally remains in a shutdown state while not converting and powers up only for conversions. Analog Devices also offers 8- and 10-bit pin-compatible solutions.

AD799x Family Features

- Specified for V_{DD} of 2.7 V to 5.5 V
- Temperature range: –40°C up to +125°C
- I²C-compatible interface
- On-chip channel sequencer

AD7991 Features

- 12-bit ADC with conversion time of 2 µs typ
- 4-channel/3-channel with reference input
- 8-/10-bit pin-compatible options
- Low power in shutdown mode: 1 µA max
- Industry's smallest package: 8-lead SOT-23



AD7991 $3.18

APPLICATIONS

- Channel monitoring
- Battery and temperature measurements
- Medical instruments
- Voltage monitoring
- Infotainment

For samples and data sheets, visit www.analog.com/V7ADC

ANALOG DEVICES

IF Diversity Receiver Addresses Cost and Size Challenges Inherent in Wireless Infrastructure Design

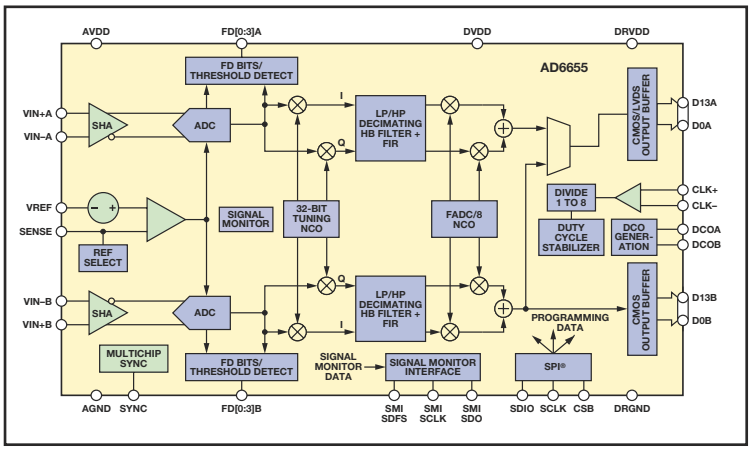
As 3G markets continue to develop, base station manufacturers need to meet the demanding performance, size, power, and cost requirements of third generation 3G standards such as CDMA2000, UMTS, TD-SCDMA, and 4G standards such as WiMAX. With these technologies, mobile communications are evolving from voice-centric services to multimedia, content-rich information services, while holding to high standards of performance, functionality, and quality of service. This migration, coupled with the variety of standards implemented in different parts of the world, poses many design challenges for telecommunications equipment makers and service providers.

Solution

ADI's new intermediate frequency (IF) diversity receiver, the AD6655, combines the industry's fastest dual, 14-bit ADC at 150 MSPS with a digital downconverter. This highly integrated solution enables efficient processing of multicarrier standards by removing the traditional interconnect issues associated with high speed data transfer from the ADC to the DDC. In addition, the device reduces BOM components count, is very low power at 600 mW/channel, has a small 9 mm × 9 mm, 64-lead LFCSP footprint, and can support multiple 3G technologies.

Online Seminar Series

"Options and Solutions for RF System Design" at *www.analog.com/onlineseminars*.



AD6655 $97.50

Purchase of licensed I²C components of Analog Devices or one of its sublicensed Associated Companies conveys a license for the purchaser under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

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BY SHREHARSHA RAO • TEXAS INSTRUMENTS

Estimating the ZigBee transmission-range ISM band

DESIGNERS OF SHORT-RANGE WIRELESS DEVICES IN THE 900-MHz AND 2.4-GHz BAND NEED TO UNDERSTAND WHAT AND HOW PARAMETERS AFFECT THE TRANSMISSION RANGE BASED ON FORMULAS AND BE ABLE TO APPLY THEM IN FORMULAS FOR STATISTICALLY CALCULATING THE PATH LOSS AND RANGE FOR BOTH INDOOR AND OUTDOOR ENVIRONMENTS.

As home, building, and industrial-automation applications go wireless, short-range wireless devices are receiving a lot of attention. Typically, these applications use either proprietary or standards-based approaches, such as ZigBee in the 900-MHz and 2.4-GHz ISM (industrial/scientific/medical) bands. With the increased popularity of short-range wireless devices, it's more important than ever for end-system designers to fully understand the range of wireless communications. This article discusses wireless propagation and develops models to estimate the path loss and range for short-range wireless devices in indoor environments. These models give system designers an initial estimate on a wireless-communication system's performance.

Before exploring range-estimation formulas, designers need to understand the wireless channel and propagation environment. The wireless-radio channel is the transmission path between the transmitter and its intended receiver. Unlike wired channels, which are stationary and predictable, wireless channels are random, time-variant, and difficult to model. So, designers need to use statistical modeling for these random channels.

Radio-wave-propagation models have traditionally focused on predicting the average received-signal strength at a given distance from the transmitter, as well as the signal's strength variability in close proximity to a location. Propagation models that predict the mean signal strength for an arbitrary transmitter-receiver separation are large-scale propagation models and are useful in estimating the transmitter's range. Conversely, propagation models characterizing the rapid fluctuations of the received-signal strength over distances of a few wavelengths are small-scale, or fading, models. This article focuses on the large-scale propagation model, which estimates the range of wireless transmission.

TABLE 1 AVERAGE SIGNAL LOSS FOR RADIO-PATH OBSTRUCTION BY DIFFERENT MATERIALS

Material Type	Loss (dB)	Frequency (MHz)
Metal	26	815
Concrete-block wall	13	815
Loss from one floor	20 to 30	1300
Loss from one floor and one wall	40 to 50	1300
6-in.-diameter metal pole	3	1300
Concrete wall	8 to 15	1300
Concrete floor	10	1300
Transmitter turning at right angle along corridor	10 to 15	1300

The free-space-propagation model predicts the received signal's strength when the transmitter and the receiver have a clear, unobstructed line-of-sight path between them. The free-space model predicts that the received-signal strength "decays" as a function of the transmitter-receiver separation distance raised to the nth power—the "power-law" function. The free-space power that the receiver's antenna receives is separated from a transmitting antenna by a distance, which the Friis free-space equation defines:

$$P_R(d) = \frac{P_T G_T G_R \lambda^2}{(4\pi)^2 d^2}, \quad (1)$$

where P_T is the transmitted power; $P_R(d)$ is the received power and is a function of the transmit-receive separation, d; G_T is the transmitter-antenna gain; G_R is the receiver-antenna gain; d is the distance between the transmitter and the receiver in meters; and λ is the wavelength in meters.

The Friis free-space equation shows that the received power "falls off" as the square of the transmitter-to-receiver separation distance. This result suggests that the received power decays with distance at a rate of 20 dB/decade.

An important term in estimating the wireless-transmission range is path loss, which represents signal attenuation in decibels. Path loss is the difference in decibels between the transmitted power and the received power at the antenna. From **Equation 1**, you can deduce the path loss as the transmitted power divided by the received power. **Equation 2** defines the path loss as:

$$P_L = 10\log\frac{P_T}{P_R} = -10\log\frac{G_T G_R \lambda^2}{(4\pi)^2 d^2}, \quad (2)$$

where P_L is path loss. To simplify **Equation 2**, assume that both the transmitting and the receiving antennas have unity gain, and this assumption results in:

$$P_L = 10\log\frac{P_T}{P_R} = -10\log\frac{\lambda^2}{(4\pi)^2 d^2}. \quad (3)$$

You can also express this **equation** in the following usable form:

$$P_L = 20\log_{10}(f_{MHz}) + 20\log_{10}(d) - 28, \quad (4)$$

or

$$P_R = P_T - P_L, \quad (5)$$

where d is the distance in meters.

The Friis free-space formula can estimate the received-power level only for values of d that are in the transmitting antenna's far field. The far field, Fraunhofer region, of a transmitting antenna is the region beyond the far-field distance, d_F. For an antenna, d_F is $2D^2/\lambda$, where D is the antenna's largest physical linear dimension. Also, d_F must be greater than D and must be in the far-field region. This path-loss formula applies only to ideal systems with clear lines of sight, and you should use it only for initial estimates.

Propagation models use the close-in distance, d_0, as the received-power reference point. You must calculate the received power, $P_R(d)$, at any distance greater than the received-power reference point with reference to $P_R(d_0)$, whose value you can predict from **equations 1** and **4**. Alternatively, you can measure it in the radio environment by taking average received power at many points from a close distance from the transmitter. You must select the close-in reference distance so that the far-field region is greater than the close-in distance.

Using this information, you can calculate the received power at any distance using the following formula:

$$P_R(d) = P_R(d_0)\left(\frac{d_0}{d}\right)^2. \quad (6)$$

The reference distance for practical systems operating at 1 to 2 GHz is 1m for indoor environments and 100m for outdoor environments.

Most RF power-level units are either in decibels referred to milliwatts or decibels referred to watts rather than absolute power levels. You can rearrange **Equation 6** as:

$$P_R(d) = P_R(d_0) + 20\log_{10}\left(\frac{d_0}{d}\right). \quad (7)$$

The following example explains these concepts. Assuming a transmitting frequency of 900 MHz, the transmit power of 6.3 mW (8 dBm), and the unity-gain transmitting and receiving antennas, determine the received power at 1200m distance in an outdoor-line-of-sight environment. For an outdoor environment, the reference distance is 100m, and you must determine the received power at 100m. The wavelength at 900 MHz is 0.33m.

TABLE 2 FAF (FLOOR-ATTENUATION FACTOR) FOR SIGNAL PENETRATION ACROSS MULTIPLE FLOORS

No. of floors	Floor-attenuation factor (dB)	Frequency (MHz)	Standard deviation (dB)
One	13.2	915	9.2
Two	18.1	915	8
Three	24	915	5.6
Four	27	915	6.8
Five	27.1	915	6.3

Using the values in **Equation 1**, you obtain

$$P_R(100) = \frac{0.0063(1)(1)(1/3)^2}{(4\pi)^2(100)^2} = 0.44\times10^{-9}\,\text{W}. \quad (8)$$

To calculate the power in decibels referred to milliwatts, you must express the power in milliwatts as:

$$P_R(100) = 0.44\times10^{-6}\,\text{mW}. \quad (9)$$

Therefore,

$$P_R(100) = 10\log(0.44\times10^{-6}\,\text{mW}) = -63.6\,\text{dBm}. \quad (10)$$

Using **Equation 7** to obtain the received power at 1200m yields:

$$P_R(1200) = P_R(100) + 20\log\left(\frac{100}{1200}\right), \quad (11)$$

and

$$P_R(1200) = -63.6\,\text{dBm} - 21.58\,\text{dB} = -85\,\text{dBm}. \quad (12)$$

Using **Equation 5**, you can verify the same value of received power.

Thus, for an ideal, unobstructed-outdoor-line-of-sight environment, the received power at a 1200m distance when the transmit power is 8 dBm is approximately −85 dBm. The actual received power will be lower because the real-world environment will likely have obstructions in the line-of-sight path or, worse, no line-of-sight path at all. For the previous example, you calculate the path loss as $P_T - P_R$. Therefore, path loss is 8 dBm − (−85 dBm) = 93 dB.

PRACTICAL PATH-LOSS FORMULAS

For any practical wireless-sensor system, it's important to know the maximum reliable data-transmission range. This wireless-system range directly depends on the link-budget parameter:

$$LB = P_T + G_T + G_R - RS, \quad (13)$$

where LB is the link budget in decibels, P_T is the transmitted power in decibels referred to milliwatts or watts, G_T is the transmitter-antenna gain in decibels, G_R is the receiver-antenna gain in decibels, and RS is the receiver sensitivity. Sensitivity is the minimum RF signal that the system can detect with an acceptable SNR (signal-to-noise ratio). **Equation 14** shows the receiver sensitivity:

$$S = -174\,\text{dBm/Hz} + NF + 10\log B + SNR_{MIN}, \quad (14)$$

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where −174 dBm/Hz is the thermal noise floor, NF is the overall-receiver-noise figure in decibels, B is the overall receiver bandwidth, and SNR_{MIN} is the minimum SNR. If the total path loss between the transmitter and the intended receiver is greater than the link budget, loss of data ensues, and communications cannot take place. Therefore, it's important for designers developing end systems to accurately characterize the path loss and compare it with the link budget to obtain initial estimations of the range.

PATH LOSS IN INDOOR CHANNELS

The indoor-radio channel differs from the outdoor channel because the indoor channel has shorter distances to cover, higher path-loss variability, and, thus, greater variance in the received-signal power. However, variability in the received-signal power is negligible for stationary wireless devices. Building layout, type, and construction materials strongly affect indoor propagation. Research classifies indoor channels as either line-of-sight or obstructed channels with varying degrees of clutter (**Reference 1**). A building's internal and external structures have a wide variety of partitions and obstacles. Partitions depend on whether the structure is a home or an office environment. Partitions in a building's structure are hard partitions, and partitions that can move and do not span to the ceiling are soft partitions. Houses typically use wood-frame partitions, whereas office buildings use soft partitions with metal-reinforced concrete between floors.

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Partitions vary widely in their physical and electrical characteristics, making it difficult to apply generic models for indoor channels. However, extensive investigations tabulate signal losses for common material types (**Table 1**). Floor-attenuation factors represent the partition loss between floors (**Table 2**). **Equation 15** shows the practical path-loss model for indoor channels using the log-distance path-loss model:

$$P_L(d) = \overline{P_L}(d_0) + 10n\log_{10}\left(\frac{d}{d_0}\right) + X_\sigma, \qquad (15)$$

where X is a zero-mean gaussian random variable in decibels and σ is standard deviation. If the devices are stationary, you can ignore the effects of X_σ. Calculating the value of path loss at a distance of 1m using **Equation 4** and plugging it into **Equation 15** results in:

$$\overline{P_L}(d) = 20\log_{10}(f_{MHz}) + 10n\log_{10}(d) - 28 + X_\sigma. \qquad (16)$$

The value of n does not vary much with frequency and depends on the surroundings and the building type (**Table 3**).

An in-building propagation model includes the effect of building type as well as obstructions. This model provides flexibility and can reduce the standard deviation between measured and predicted path loss to approximately 4 dB compared with 13 dB when you use only a log-distance model. **Equation 17** represents the attenuation-factor model:

TABLE 3 PATH-LOSS EXPONENT AND STANDARD DEVIATION IN DIFFERENT BUILDINGS

Building	Frequency (MHz)	Path-loss exponent, n	Standard deviation (dB)
Retail store	914	2.2	8.7
Grocery store	914	1.8	5.2
Office, hard partition	1500	3	7
Office, soft partition	900	2.4	9.6
Office, soft partition	1900	2.6	14.1
Factory, line of sight	1300	2	3
Suburban, indoor street	900	3	7
Factory, obstructed path	1300	3.3	6.8

$$P_L(d) = 20\log_{10}(f_{MHz}) + 10n_{SF}\log_{10}(d) - 28 + FAF, \qquad (17)$$

where n_{SF} represents the path-loss exponent value for the same floor measurement and FAF is the floor-attenuation factor (**Table 3**). You can determine the FAF value from (**Table 2**). The following examples demonstrate how to use the foregoing **tables** and **equations**: For example, calculate the path loss for an outdoor free-space environment at a distance of 1200m at 915 MHz and 2.4 GHz. Using

$$20\log_{10}(f_{MHz}) + 20\log_{10}(d) - 28, \qquad (18)$$

you can deduce P_L at:

$$915\ MHz = 20\log_{10}(915) + 20\log_{10}(1200) - 28 = 92.8\ dB, \qquad (19)$$

and P_L at:

$$2400\ MHz = 20\log_{10}(2400) + 20\log_{10}(1200) - 28 = 101.2\ dB. \qquad (20)$$

Propagation at a higher frequency results in higher path losses, which results in the reduction of wireless-transmission ranges at higher frequencies: For example, wireless devices operating in the 2.4-GHz range suffer from an approximately 8.4-dB reduction in path loss compared with a device operating at 915 MHz in an outdoor, free-space environment.

In another example, using the information in **Table 2**, calculate the path loss for an indoor-office environment with hard partitions at a distance of 100m at 915 MHz and 2.4 GHz across the same floor and three floors. For the same floor, from **Table 3**, the average path loss is 3 dBm. Using this value of n=3 in:

$$20\log_{10}(f_{MHz}) + 10\log_{10}(d) - 28 + X_\sigma, \qquad (21)$$

yielding P_L at:

$$915\ MHz = 20\log_{10}(915) + 10(3)\log(100) - 28 + X_\sigma = 91.2\ dB, \qquad (22)$$

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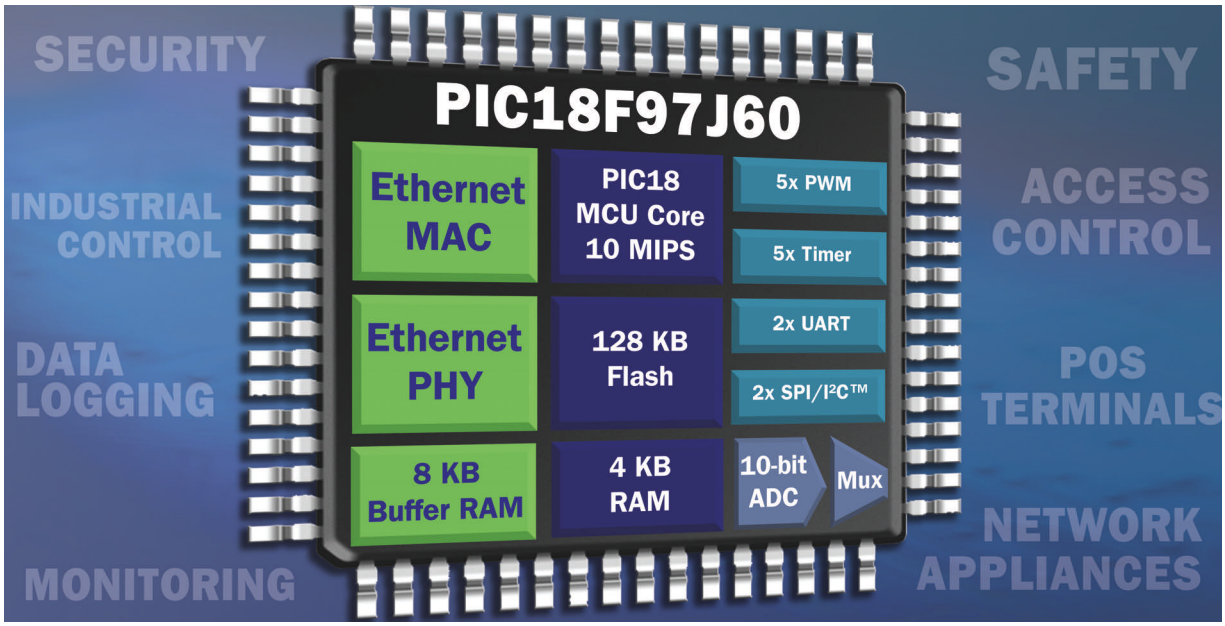

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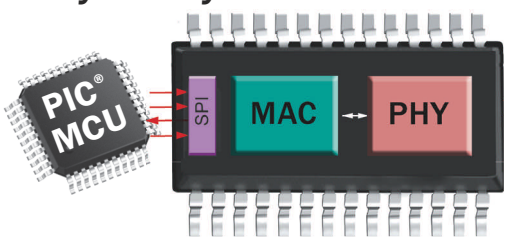

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where $\sigma=7$ dB. And P_L at:

$$2400\ \text{MHz}=20\log_{10}(2400)+10(3)\log(100)-28+X_\sigma=99.6\ \text{dB}, \quad (23)$$

where $\sigma=14$ dB.

From **Table 2**, you can calculate the FAF for propagation for three floors as approximately 24 dB with a standard deviation of 5.6 dB. Using the information in

$$20\log_{10}(f_{MHz})+10n\log_{10}(d)-28+X_\sigma, \quad (24)$$

you can deduce P_L at:

$$915\ \text{MHz}=20\log_{10}(915)+10(3)\log_{10}(100)-28+24=115.2\ \text{dB}, \quad (25)$$

where $\sigma=5.6$ dB, and P_L at:

$$2400\ \text{MHz}=20\log_{10}(2400)+10(3)\log_{10}(100)-28+24=123.6\ \text{dB}, \quad (26)$$

where $\sigma=5.9$ dB.

In a third example, estimate the transmission range at 915 MHz for the above two examples assuming a system with unity-gain transmitting and receiving antennas, a transmitting power of 8 dBm, and a receiver sensitivity of −100 dBm. The system's link budget is $8-(-100)=108$ dB.

It's a good idea to have a link-budget margin of approximately 10 dB to account for the standard deviations in the path-loss formulas. Thus, the available link budget is 98 dB, which exceeds the path loss of 92.8 dB from the first example; therefore, you can consider 1200m to be outdoor range. In the indoor environment, path loss is 91.2 dB, and the available link budget is approximately 98 dB, assuming a 10-dB margin, which exceeds the path loss. Therefore, you can consider 100m to be the indoor range of that system. EDN

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1 Rappaport, Theodore S, *Wireless Communications Principles and Practice*, Prentice Hall, 2001.

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Designing medical devices for isolation and safety

OPTOCOUPLERS, ALONG WITH SOUND DESIGN PRACTICES, PROVIDE EFFECTIVE ISOLATION FOR MEDICAL EQUIPMENT AND PROTECT PATIENTS FROM POTENTIALLY DANGEROUS LEAKAGE CURRENTS.

The use of ac-line-powered medical diagnostic, measurement, and treatment equipment potentially exposes patients and even caregivers to the risk of electrical shock, burns, internal-organ damage, and cardiac arrhythmias directly due to leakage current resulting from improper grounding and electrical isolation. The electrical conductivity of body fluids and the presence of various conductive solutions and gels in the patient care make the treatment environment even more potentially dangerous. The use of gels substantially reduces the normally high resistance of the skin—greater than 50Ω. A second significant hazard results from potential electrical emissions among the diagnostic and treatment devices, which can degrade the performance of other nearby medical devices. As a result, many regulations from agencies ranging from the US FDA (Food and Drug Administration), the EU (European Union), and other safety and regulatory bodies ensure that these medical devices comply with the safety standards.

Standard IEC (International Electrotechnical Commission) 60601-1 defines medical-equipment electrical-safety conditions necessary to protect patients, operators, and the surroundings. Other standards define more than just safety requirements. For example, the IEC 60601-1-x collateral-standard series deals with issues such as EMC (electromagnetic compatibility), X-ray protection, and programmable electrical medical systems. EMC is indeed an important criterion for medical equipment because the equipment cannot be a source of EMI (electromagnetic interference), which could prevent accurate operation of other medical equipment and must be immune to potential EMI in the operating environment. Since November 2005, medical equipment has had to comply with the updated IEC 60601-1-2:2001 EMC standard.

In the portions of the medical equipment transmitting digital data, designers can isolate sensitive circuitry or patients

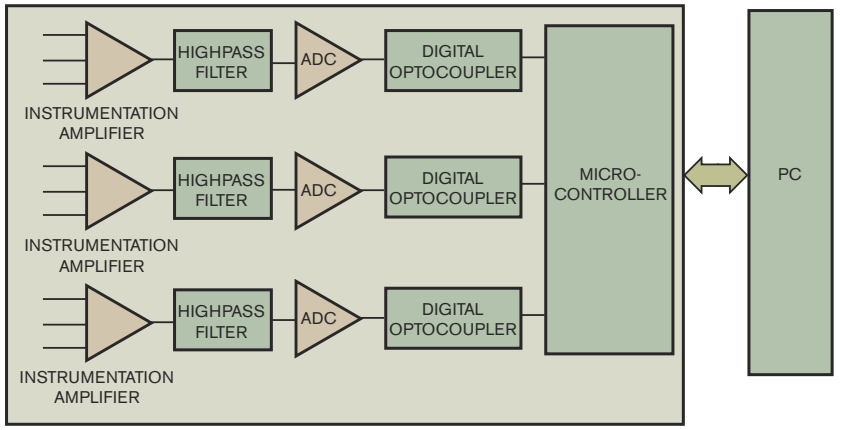

Figure 1 A front-end module in an ECG machine indicates the use of galvanic isolation devices, or optocouplers, to isolate patient electrodes from the machine's electronics.

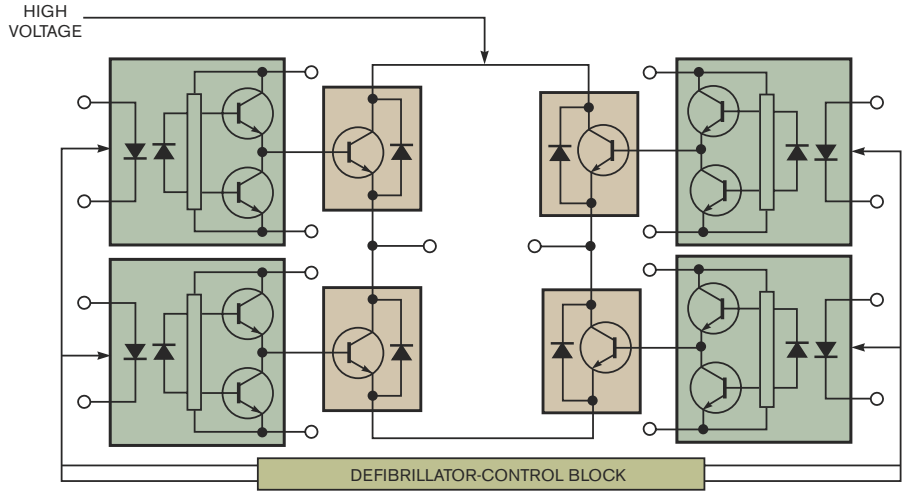

Figure 2 A defibrillator device uses optical isolation to separate the high-voltage-pulse section from the device's low-voltage control electronics.

from high-voltage environments using optocoupler- or transformer-based approaches. Optocoupler-based techniques have in the past been able to support only limited data rates, which led to the use of transformer-based isolation. This approach provided the requisite data rates but generally required more components taking up more space on a PCB (printed-circuit board) and a more complex design. This situation has changed with the introduction of optocouplers capable of higher data rates and improved timing characteristics.

REINFORCED GALVANIC ISOLATION

Unlike functional isolation, reinforced isolation both protects from electric shock and ensures that a design is fail-safe—a mode of system termination that automatically leaves system processes and components in a secure state when a failure occurs or when a system detects a failure (**Reference 1**). This feature is critical for medical equipment, such as an ECG (electrocardiograph) system or a defibrillator (**figures 1** and **2**, respectively). Optocouplers providing reinforced isolation are certified under IEC/EN/DIN (Deutsches Institut für Normung) EN 60747-5-2, which is an international standard for optically isolated semiconductor components.

To meet the IEC-60601-1 medical standards' insulation requirements, optocouplers must have UL (Underwriters Laboratories) 1577 or IEC 60747-5-2 certification and must meet component-creepage, external-clearance, and test-voltage requirements depending on the insulation level of the interface. The certification defines creepage distance as the shortest surface path over a solid dielectric between two galvanically isolated conductors. The external-clearance distance is the shortest distance through air, or "line-of-sight" distance, between two galvanically isolated conductors.

When operating at working voltages higher than 50V rms, 71V peak, or dc and for reinforced-insulation-level applications, the DTI (distance through isolation) must be at least 0.4 mm (**Reference 2**). The DTI is the internal-clearance distance between conductors inside an insulation device, such as that between the LED and the detector inside an optocoupler or optoisolator (**Figure 3**). To illustrate the typical specification requirements for medical equipment, **Table 1** summarizes IEC 60601-1. **Table 2** shows specifications of optocouplers that meet the IEC 60601 requirements for insultion. The Type 1 requirement targets devices operating at less than 70V, which require only basic insulation, and the Type 2 requirement targets equipment that operates at voltages greater than 70V and thus requires reinforced insulation or a similar level of protection.

TABLE 1 IEC 60601-1 SAFETY-STANDARD REQUIREMENTS

Working voltage[1] (V_{DC})	Working voltage[1] (V rms)	Insulation type	Creepage (mm)	Clearance (mm)	Distance through insulation[3] (mm)	Test voltage (V rms for 1 minute)
17	12	Basic[2]	1.7	0.8		500
		Reinforced[2]	3.4	1.6		800
34	30	Basic	2	1		500
		Reinforced	4	2		800
85	60	Basic	2.3	1.2		765
		Reinforced	4.6	2.4	0.4	1224
177	125	Basic	3	1.6		1000
		Reinforced	6	3.2	0.4	1733
354	250	Basic	4	2.5		1494
		Reinforced	8	5	0.4	2390
566	400	Basic	6	3.5		1864
		Reinforced	12	7	0.4	2982
707	500	Basic	8	4.5		2060
		Reinforced	16	9	0.4	3000
934	660	Basic	10.5	6		2343
		Reinforced	21	12	0.4	3000
1061	750	Basic	12	6.5		2508
		Reinforced	24	13	0.4	3000
1414	1000	Basic	16	9		2868
		Reinforced	32	18	0.4	3000

[1] Working voltage is the voltage to which the relevant insulation is subjected in normal use and rated supply voltage, whichever is greater.
[2] Class 1 equipment uses basic insulation; Class 2 equipment uses reinforced insulation.
[3] The IEC 60601-1, third edition only recently instituted the DTI requirements for medical equipment, and they are identical to the DTI requirements from IEC 60950 (information-technology equipment).

To meet EMC requirements in IEC 60601-1-2, medical devices must be immune to ESD (electrostatic discharge), RFI (radio-frequency interference) from nearby transmitters and other sources, and power disturbances that cause device malfunctions (**Table 3**). In addition to these requirements, the device's own emissions, through either conduction or radiation, may interfere with licensed communications sources or other equipment and thus should be minimal (**Table 4**). The devices must have ESD protection as high as 8 kV through air and 6 kV on contact. They must be immune at frequencies of 80 MHz to 2.5 GHz and 3V/m of RF electromagnetic force for non-life-supporting equipment and 10V/m for life-supporting equipment. These tests are essential performance criteria, in that they cannot have any component failures, changes in programmable parameters, resetting to factory defaults, changes of operating modes, or false alarm. Properly designed optocouplers are more immune to EMI than are

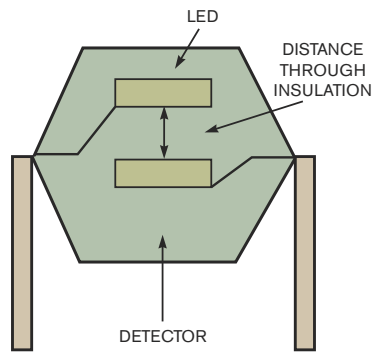

Figure 3 The distance through insulation is the internal-clearance distance between conductors in an insulation device.

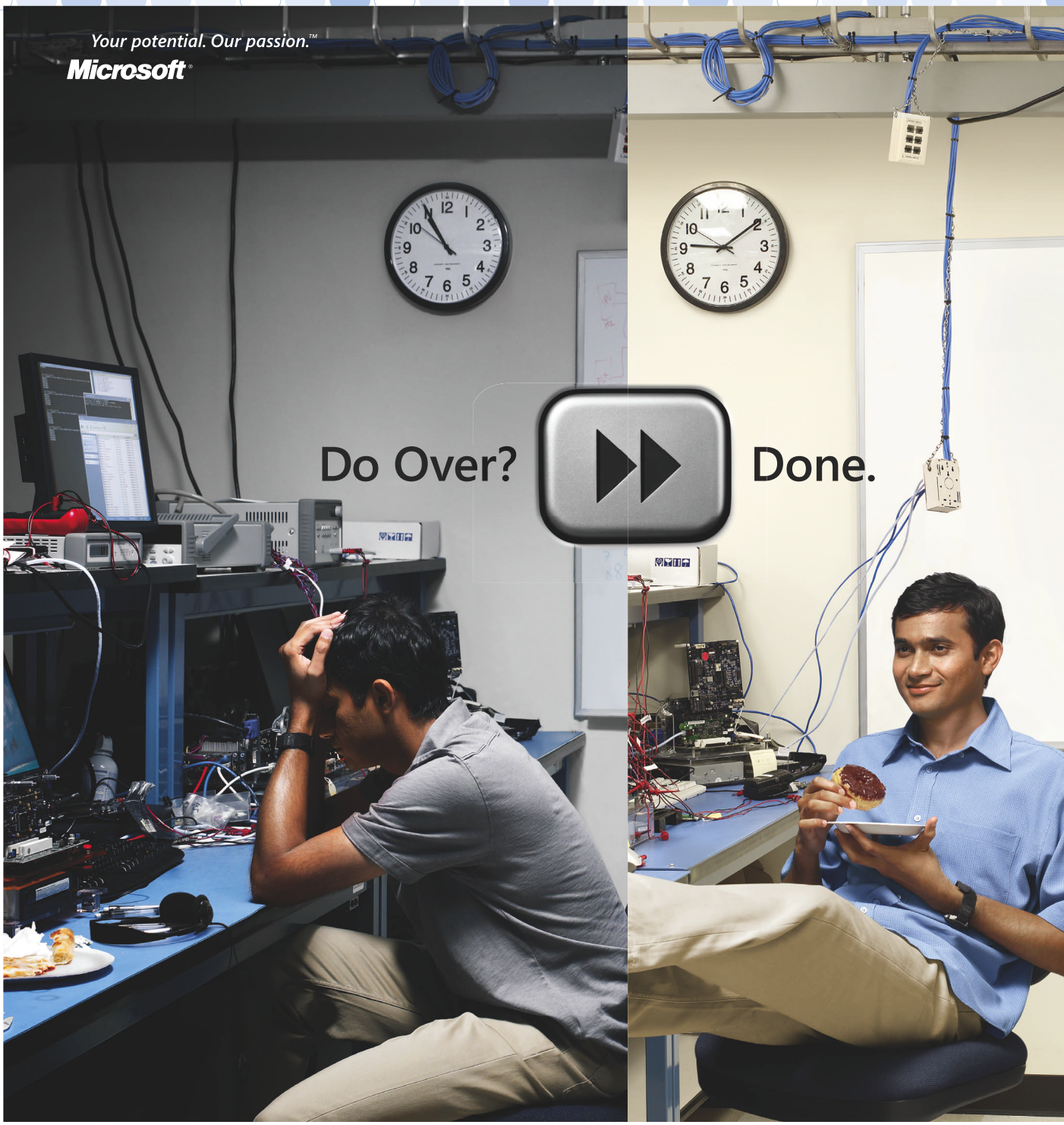

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TABLE 2 IEC 60601-1-COMPLIANT INSULATION

	Type 1 requirements	Type 2 requirements	Example of optocouplers meeting Type 1[1]	Example of optocouplers meeting Type 2[2]
Interface type	Less than 70V dc	More than 70V dc	Less than 70V dc	More than 70V
Insulation type	Basic	Double	Reinforced	Reinforced
Creepage (over-surface spacing)	4 mm	8 mm	4 mm or more	10 mm
External clearance (through-air spacing)	2.5 mm	5 mm	4 mm or more	9.6 mm
Distance through isolation (DTI)	NA	0.4 mm	0.08 mm or more	1 mm
Dielectric-strength level	1.5 kV	4 kV	3.75 kV or more	5 kV
Standard required	UL 1577 and IEC 60747-5	UL 1577 and IEC 60747-5	UL 1577 and IEC 60747-5	UL 1577 and IEC 60747-5
Example	Patient-acquisition module	Electrocardiograph device	Patient-acquisition module	Electrocardiograph device

Reproduced with permission of Gary Powalisz, GE Healthcare.
[1] Example: Avago Technologies HCPL-xxxx (HCPL-0723), ACPL-xxxL series.
[2] Example: Avago Technologies HCNWxxx (HCNW2611) series. Certain Avago Technologies optocouplers (wide-body-package series: HCNWxxx as well as DIP-8 package with option -020) offer a minimum isolation voltage of 5 kV rms/1 minute per UL 1577 and CSA component acceptance notice No. 5.

TABLE 3 IEC 60601-1-2 IMMUNITY REQUIREMENTS

Immunity test	IEC 60601 test level
Electrostatic discharge (ESD) IEC 61000-4-2	±6 kV contact ±8 kV air
Electrical fast transient/burst IEC 61000-4-4	±2 kV for power-supply lines ±1 kV for I/O lines
Surge IEC 61000-4-5	±1 kV lines to lines ±2 kV lines to lines
Voltage dips, short interruptions, and voltage variations on power-supply-input lines IEC 61000-4-11	Less than 5% U_r (greater than 95% dip in U_r) for 0.5 cycle 40% U_r (60% dip in U_r) for five cycles 70% U_r (30% dip in U_r) for 25 cycles Less than 5% U_r (greater than 95% dip in U_r) for 5 sec
Power frequency (50/60 Hz) magnetic field IEC 61000-4-8	3A/m

NOTE: U_r is the ac-mains voltage before application of the test level.

TABLE 4 IEC 60601-1-2 EMI REQUIREMENTS

Emissions test	Guidance
RF emissions CUSPR 11	To measure the electromagnetic energy that is generated internally for it to perform its intended function that may interfere with any nearby equipment.
Conducted emissions CUSPR 11	To measure the effects of emissions conducted onto ac-power lines.
Harmonic emissions/ flicker emissions IEC 61000-3-3	To measure the harmonic frequency injected into the public mains network for equipment and systems with a rated input current as high as 16A per phase and that are intended to be connected to it.
Voltage fluctuations/ flicker emissions IEC 61000-3-3	To measure the emissions, fluctuations, and flicker injected into the public mains network for equipment and systems with a rated input current as high as 16A per phase and that are intended to be connected to it.

other isolation devices, such as transformers, because optocouplers transmit signals through optical radiation between the LED light source and the photodiode. Tests on optocouplers have demonstrated their ability to withstand ESD voltage as high as 11 kV (**Reference 1**). Optocouplers are effective in passing the intended differential-mode signals and blocking the unintended common-mode currents and resulting ground-offset voltage that can result from ground-loop currents.

In summary, available optocouplers clearly meet the general medical-safety requirement that IEC 60601-1 defines. In addition, optocouplers provide excellent EMI and emit no electromagnetic waves, which is now an important measure for medical-equipment certification. EDN

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Q. Must I consider high frequency issues when driving a slow ADC?

A. Because things are not always what they seem. Consider the quagga — the last one died in Amsterdam zoo on the 12th August 1883 and they have long been considered extinct. Recent genetic research on the remains of a number of quaggas show that they were not a separate species, but a pattern variant of the basic African plains zebra. There is a good chance that a selective breeding program can resurrect the quagga, allowing it to be returned to its former habitat. This project is now in hand and the results, which I hope to have seen by the time you read this, are very encouraging.

Similarly a "dc" ADC input is often nothing of the sort. The analog inputs of many different types of ADCs contain switched capacitors. Sometimes they are buffered with amplifiers, but generally the circuits driving the ADC input terminals must tolerate the fast transient currents that flow as the capacitors are switched. The repetition rate of these current pulses may be the system sampling clock frequency, but sometimes it is the much higher conversion clock frequency of the ADC. If the input interface cannot tolerate these fast current pulses, there is a serious risk that the system will malfunction and suffer from nonlinearity, or even missing codes.

We can handle the problem in two ways. The simplest is to place a capacitor between the ADC input and ground, allowing the transient currents to flow in the capacitor rather than in the drive circuit. The alternative is to use a driver/interface circuit that can tolerate fast current transients.

If we use the capacitor, we may be reducing our system's frequency response. It is important, if we use this approach, to ensure that the circuitry driving the ADC input will be stable with the additional capacitive load, and that the system bandwidth will still be as large as necessary.

If we choose to use a drive circuit capable of handling the transients without an added capacitor, we must confirm (probably by experiment — spice macro models may not be detailed enough to predict the effect of such fast transients) that the amplifier or other driver will handle the transients over the whole input dynamic range, as the pulse amplitude may well vary with input level.

It is also very important to remember that the reference input of an ADC has the same structure as the signal input — and may have similar transients. The load capacitor of the reference IC normally prevents adverse effects — but some voltage references are promoted as "not needing output capacitors." This may be true when they are used with resistive loads, but is certainly not true when these transient currents are present.

To learn more about circuitry driving the ADC input,
Go to: http://rbi.ims.ca/5391-101

Contributing Writer James Bryant has been a European Applications Manager with Analog Devices since 1982. He holds a degree in Physics and Philosophy from the University of Leeds. He is also C.Eng., Eur.Eng., MIEE, and an FBIS. In addition to his passion for engineering, James is a radio ham and holds the call sign G4CLF.

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Reducing power consumption in battery-powered applications

USING THE LOWER POWER MODES OF ADVANCED MICROCONTROLLERS MEANS LESS BATTERY DRAIN IN PARKED AUTOMOBILES AND LONGER BATTERY LIFE IN PORTABLE CONSUMER PRODUCTS.

Automotive-electronics content is expanding at an ever-increasing pace. Today, an average car has 25 to 35 microcontrollers; approximately half of those are 8-bit units. High-end vehicles can easily have 80 or more microcontrollers. With rising energy costs fueling an explosion of hybrid technologies and car buyers demanding more comfort features and conveniences, automakers look to electronics for the solutions. This search translates to a dramatic rise in the need for computing power under the hood and in the cabin. The system challenge that all that computing power creates is a greater demand for electrical power. Because increasing the electrical capacity of the car generally adds weight and reduces fuel economy, the alternative is to either use less power or make more efficient use of the available power in the car.

In cars, an alternator supplies 100A or more to handle the loads, so saving a few microamps may seem unimportant. In fact, the biggest concern for saving power in the automotive market is for key-off modes, which stay on when the ignition key is off and the car is parked. In many cases, the microcontroller is the largest consumer of power in the key-off mode, rivaled only by wireless communications, such as the transmitter/receiver. The power consumption is a function of how frequently you power up the microcontroller and what type of operation it is performing. These microcontrollers must wake up periodically from a sleep mode based on a very-low-power oscillator. They quickly come up to operation, perform a required function, and then go back to sleep. A good example is a keyless-entry system in the body controller. This system wakes up periodically to see whether the key fob has sent a signal to open the doors.

In the key-off mode, automotive and consumer-electronics applications are similar in that they are both battery-powered. In portable electronics, power consumption is a major design consideration because it directly impacts battery life and the useful operation of the product. Fortunately, with the latest microcontrollers, designers can reduce power consumption, and the same principles apply to any power-conscious application.

TABLE 1 VOLKSWAGEN GOLF TRENDS

Volks-wagen model	No. of modules	Total vehicle sleep current (mA)	Sleep current per module (mA)
Golf I	Three	8.3	2.766
Golf II	Five	10.5	2.1
Golf III	11	16.2	1.473
Golf IV	18	21.3	1.183
Golf V	25	15.4	0.618

Historically, at the module level, the maximum current draw under a key-off situation was 1 mA. With the increasing number of modules and loads that are active during the key-off mode, most carmakers are implementing or considering a maximum current draw of a fraction of this level. For example, as **Table 1** shows, at Volkswagen, the initial Golf had three modules (**Reference 1**). The number increased to five, 11, 18, and, finally, 25 in the current Golf V model. The **table** also shows the corresponding changes in total vehicle sleep current.

Many of the largest gains in efficiency will be in comfort and convenience systems, in which the predominant hardware architecture is the 8-bit microcontroller. These systems have a

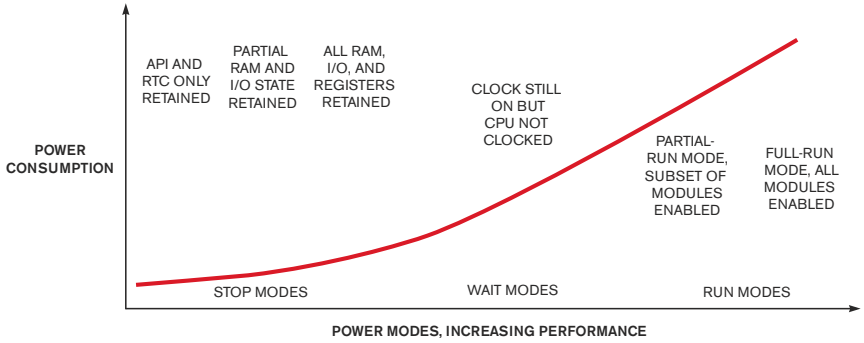

Figure 1 Flexible low-power modes allow progressively lower power consumption as active circuitry's performance decreases.

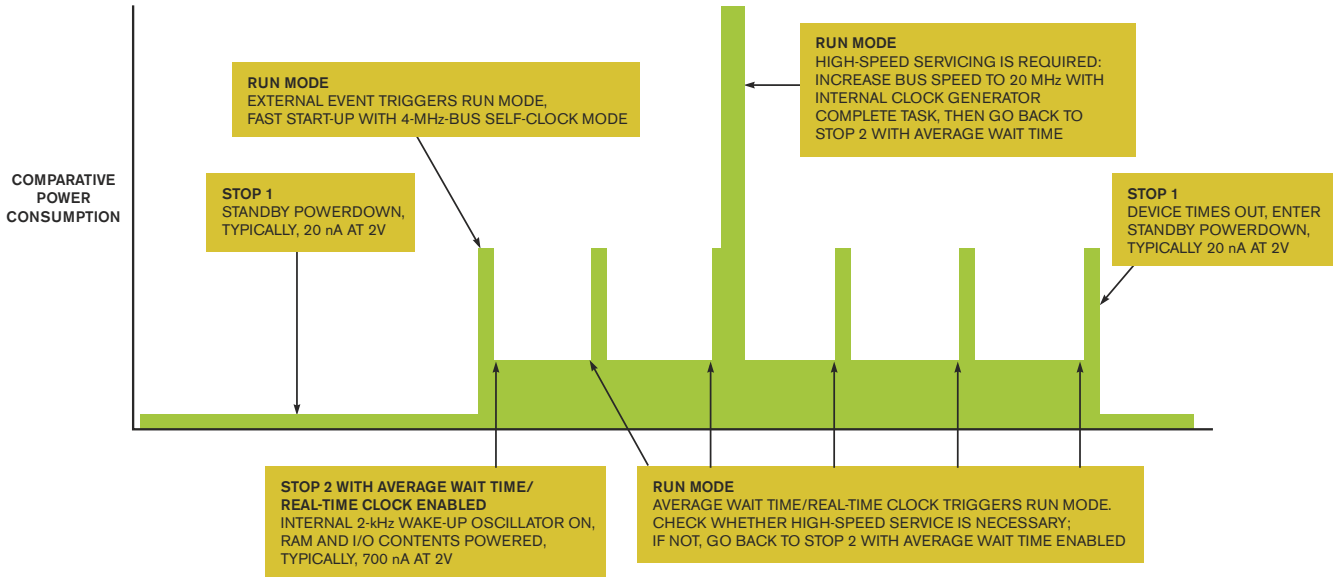

Figure 2 The power-consumption profile for stop and run modes includes a periodic wake-up.

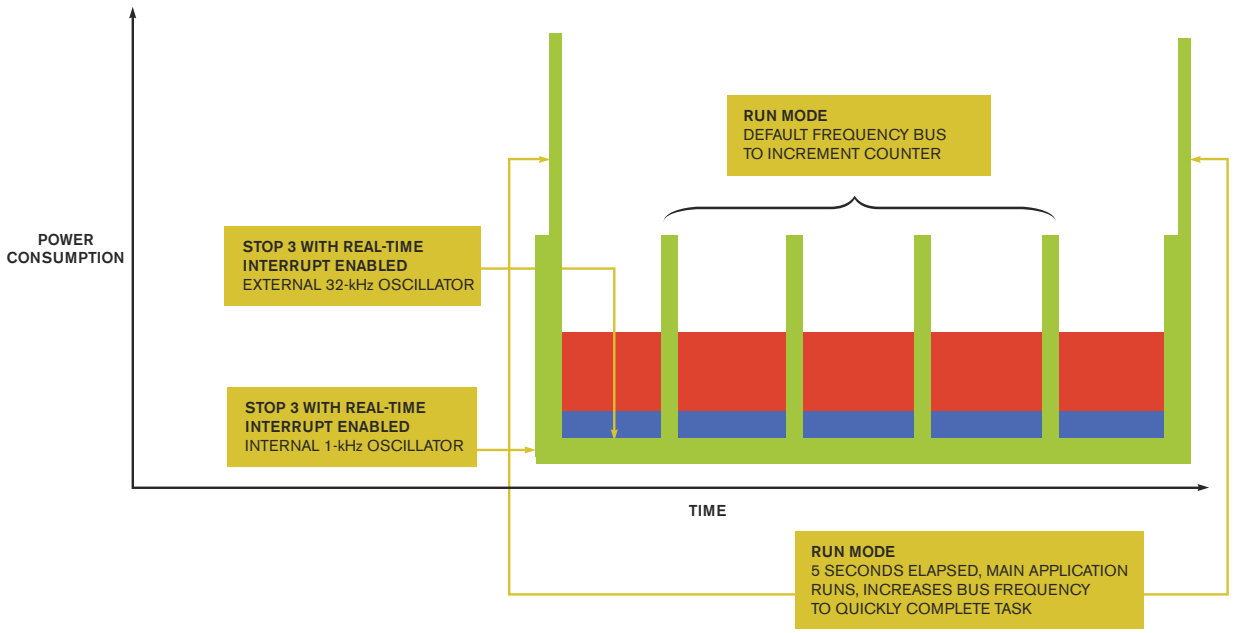

Figure 3 Extend battery life with clock management by implementing periodic wake-up and using a lower clock frequency in the run mode to reduce the average power consumption.

relatively large number of electronic components, and automakers continue to add more comfort and convenience features to a wider number of vehicle platforms. Depending on the design, the microcontroller can be a significant or a small part of the problem. With some of the latest microcontroller considerations for power, the microcontroller can become a part of the solution and provide the means to satisfy lower current requirements. This approach requires implementing the power-saving features of the next generation of 8-bit microcontrollers.

DECREASING POWER CONSUMPTION

Highly customizable features, such as variable clock speeds and multistage power-down modes, allow system designers to optimize microcontroller performance to suit not only the computing requirements of the application, but also the increasingly important power budget. More advanced clock generation also allows the user to choose how the microcontroller generates clocks to maximize the performance for a given power-consumption level. Periodic wake-up capabilities and the ability to wake up the microcontroller based on network communications or other outside signals allow the device to remain switched off until a user needs it, further extending power savings. These low-power options couple with system-protection features, such as low-voltage detection, which ensure that the application continues to operate safely while running on minimal power. These advanced capabilities hold

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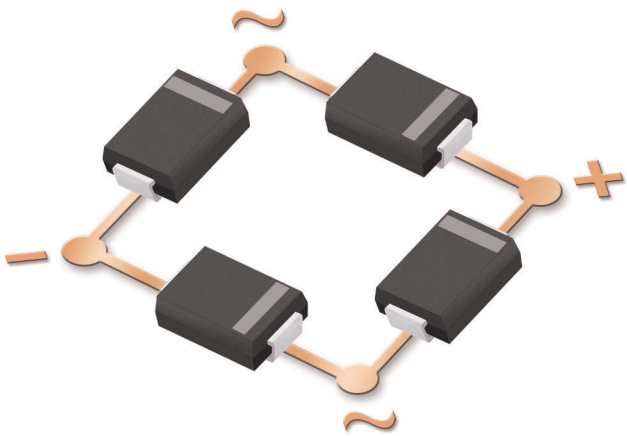

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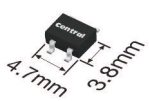

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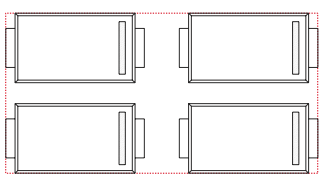

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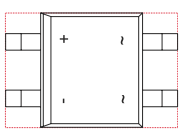

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The traditional high-level power strategies still apply. First, turn off power-consuming circuitry whenever possible, and, second, minimize the operating frequency of the system under all conditions. The newest microcontroller designs include more options for the system designer to reduce power consumption in many of the available modes. Specific modes allow the system designer to reduce power whenever possible by switching on only the necessary portions of silicon.

The modes include several stop or deep-sleep states; an intermediate wait or doze state; a modified run mode, which is a subset of microcontroller awake; and run mode, when the chip is fully awake (**Table 2**). Consumer and industrial applications use the Stop 1 mode, which is not available for automotive microcontrollers that operate at 5V. The consumer and industrial applications typically have lower operating voltages (**Reference 2**). The lowest power-consumption mode, Stop 1, is basically a shutdown mode, with a typical drain-to-drain current as low as 20 nA at 2V. This mode leaves only active circuitry, such as an interrupt pin or a pin input, powered to allow the unit to wake up. In this state, the microcontroller wakes up on an external event, edge, or level trigger. The trade-offs of this mode are that is loses RAM content, it resets all register contents, and it puts the I/O pins in the reset state.

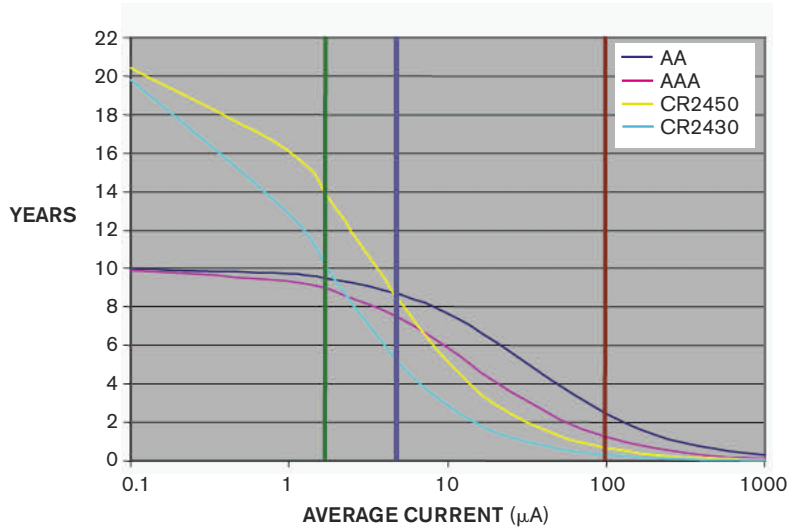

Figure 4 Reducing the average current draw has different impacts on battery life. The lowest levels of stop-, wait-, and run-mode current maximize battery life to meet 10-year operating-life goals.

In a partial power-down mode, such as Stop 2 with a drain-to-drain current as low as 400 nA at 2V, the microcontroller wakes up with an IRQ (interrupt request), reset, or internal RTI (real-time interrupt) but does not lose the RAM contents, and the I/O states are latched. The RTI can wake up the microcontroller without the occurrence of an external event. One limitation is that the register values are reset; however, you can save those values to RAM and restore them.

Another partial power-down mode, such as Stop 3 with a typical drain-to-drain current as low as 500 nA at 2V, is comparable with earlier microcontroller stop modes in that wake-up occurs with any active interrupt, including IRQ, KBI (keyboard interrupt), LVD (low-voltage detection), RTI, or reset. In addition to retaining RAM and register values without requiring initialization of peripherals, the system can use an external clock as a high-accuracy input into the RTI. The trade-off for this mode is higher current draw.

Because the CPU is the most power-hungry block on the microcontroller, you should switch it off as often as possible. To increase the number of times and situations in which you can turn them off, microcontrollers may employ a number of autonomous peripherals that require no CPU to operate. Key autonomous peripherals include the RTI, which allows the microcontroller to recover from a very-low-power state at selectable time intervals, and an RTC (real-time clock), which allows timekeeping functions in a very-low-power state. In addition, the ADC can perform continuous conversion while running in low power and trigger a wake-up when the signal reaches a user-defined level.

The RTI and ADC are parts of the fast-wake-up mechanisms that allow the microcontroller to more frequently enter stop modes at the lowest power-consumption level. These blocks increase the speed at which the device can recover from low-power modes and start execution. Once a clock is present, reconfiguration and non-timing-critical operations can start. However, very fast wake-up requires an on-chip IRC (internal reference clock), which enables almost immediate operation.

A variety of low-power-clock sources provide system designers options in start-up time and accuracy for lowering power consumption depending on the system's performance requirements (**Table 3**). The ability to implement variable clocking allows throttling back the frequency for lower current and powering up the clock rate to full speed when math-intensive computing is required.

With the new power-savings tools, designers have greater flexibility in making power-versus-performance decisions

TABLE 2 STOP MODES

Mode	CPU, digital peripherals, flash	RAM	Interactive computer graphics	Arrival-time difference	Keyboard interrupt	Regulator	I/O pins	Real-time interrupt
Stop 1	Off	Off	Off	Disabled	Off	Off	Reset	Off
Stop 2	Off	Standby	Off	Disabled	Off	Standby	States held	Optionally on
Stop 3	Standby	Standby	Standby	Disabled	Optionally on	Standby	States held	Optionally on

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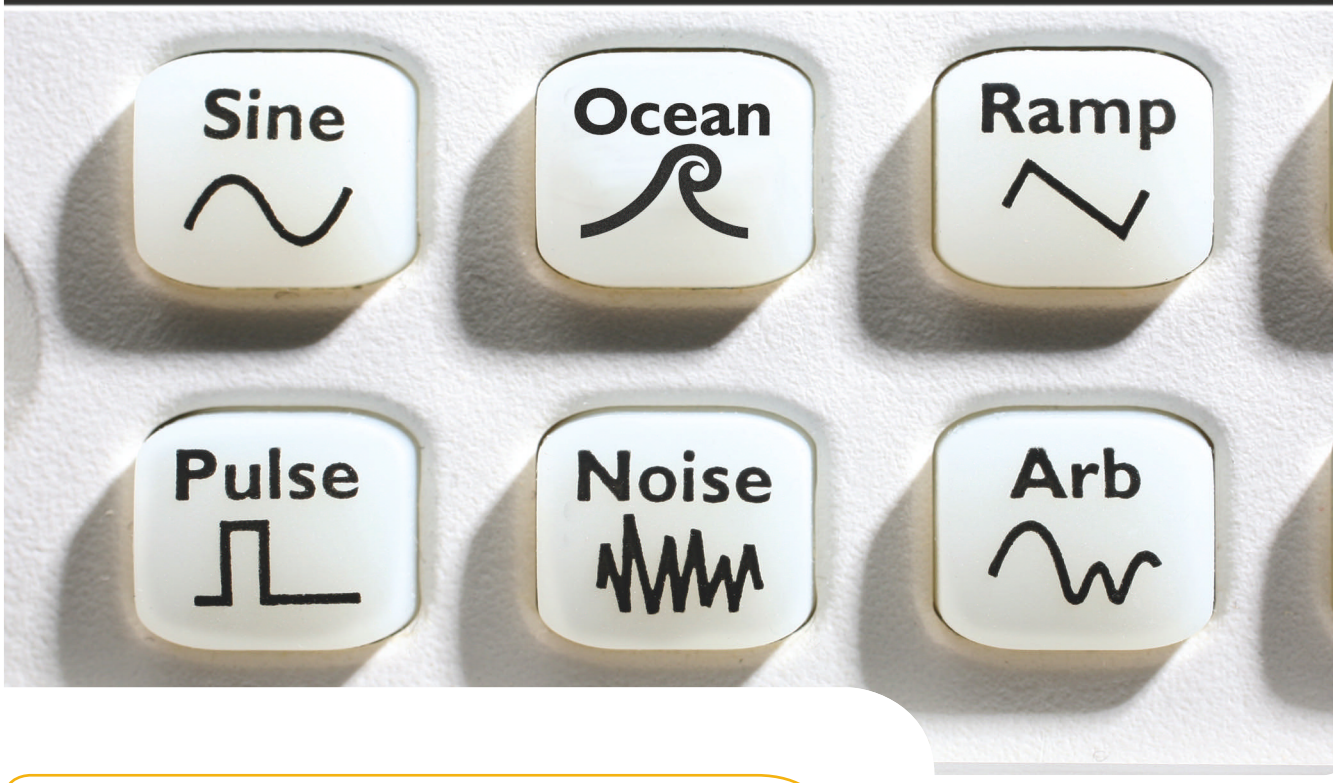

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(**Figure 1**). The **figure** identifies power modes with increasingly higher power consumption in stop, wait, and run modes. This flexibility leads to lower power consumption with a properly implemented power-management strategy. One of the strategies for reduced power consumption is periodic wake-up, which couples with the power-management modes (**Figure 2**). Even microcontrollers without an extremely low-power mode can extend battery life using a power-management scheme that uses other available stop modes (**Figure 3** and **Reference 3**).

From a systems approach, analog power-management ICs can augment the power savings in the microcontroller portion. Freescale calls these power-management chips SBCs (systems base chips), which have many aspects and variations. The fundamental pieces include voltage regulation; input- and output-drive circuitry; and, frequently, a physical layer for the communications protocol, such as a CAN (controller-area-network) or LIN (local-interconnect-network) transceiver (**Reference 4**). The key aspect is the voltage regulation for the microcontroller with a built-in communication module. With the combination of one analog IC and the microcontroller, you can put the entire system into the sleep mode with the microcontroller's power off and the regulator shut down to save even more power.

TABLE 3 CLOCK SOURCES AND THEIR ATTRIBUTES

Clock source	Start-up time	Power	Accuracy
Internal reference	Less than 100 µsec	Low	Less than 2%
Internal reference with frequency-locked loop	Less than 100 µsec	Low	Less than 2%
External reference	Milliseconds	Medium	Crystal
External reference with frequency-locked loop	Milliseconds	High	Less than 1%
External reference with phase-locked loop	Milliseconds	High	Less than 1%

Network activity turns the regulator back on, which powers up the microcontroller, allowing the system to perform the required operations. This approach saves the most current because it involves advanced power-saving capabilities, and designers can do several tricks to save even more power.

One automotive application with similar requirements to those of consumer products is the TPMS (tire-pressure-monitoring system). With the complete electronic system, including the microcontroller, sensors, transmitter/receiver, and the battery mounted inside the tire, a TPMS works just like any other battery-powered device—except that the user cannot replace the battery. This automotive application and others like it

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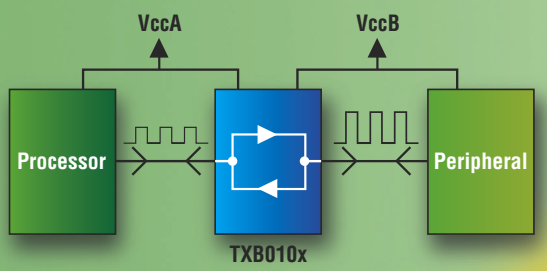
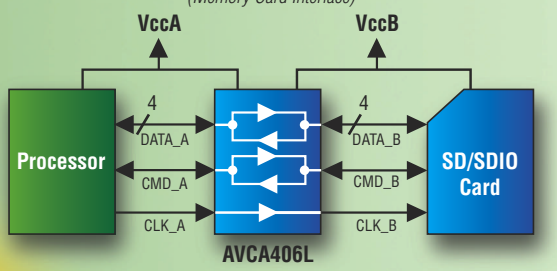
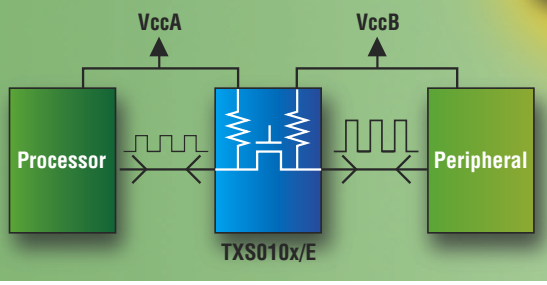


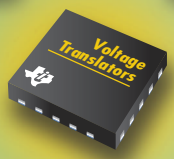
Application-Specific Translators

(Memory Card Interface)

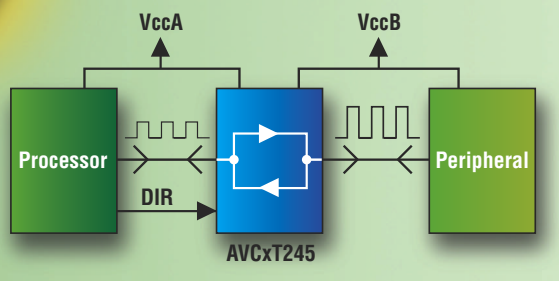


Auto-Direction-Sensing Translators for Open-Drain Applications





Dual-Supply-Configurable Translators



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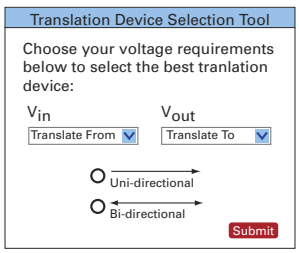
Auto-Direction Sensing Translators*					
TXS0102	2	1.65 to 3.6	2.3 to 5.5	8-kV HBM	8-bump WCSP
TXS0104E	4	1.65 to 3.6	2.3 to 5.5	10-kV Air Gap Discharge (IEC)	12-ball BGA
TXB0104	4	1.2 to 3.6	1.65 to 5.5	15-kV HBM	12-ball BGA
TXB0108	8	1.2 to 3.6	1.65 to 5.5	15-kV HBM	20-ball BGA
Application-Specific Translators (Memory Card Interface)					
AVCA406		1.4 to 3.6	1.4 to 3.6	15-kV Air Gap Discharge (IEC)	48-ball VFBGA
AVCA406L		1.2 to 3.6	1.2 to 3.6	6-kV HBM	20-ball VFBGA
CF4320H		1.65 to 3.3	3.3 to 5	15-kV HBM	114-ball LFBGA
Dual-Supply Configurable Translators*†					
SN74AVC1T45	1	1.2 to 3.6	1.2 to 3.6	2-kV HBM	6-bump WCSP
SN74AVC2T45	2	1.2 to 3.6	1.2 to 3.6	8-kV HBM	8-bump WCSP
SN74AVC8T245	8	1.2 to 3.6	1.2 to 3.6	8-kV HBM	24-pin QFN
SN74AVC16T245	16	1.2 to 3.6	1.2 to 3.6	8-kV HBM	56-ball VFBGA
SN74AVC32T245	32	1.2 to 3.6	1.2 to 3.6	8-kV HBM	96-ball LFBGA

** Other bit-width options available. † Bus Hold feature available.*



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demand the maximum effort to reduce microcontroller-power consumption. The rule of thumb in a TPMS is a 10-year battery life. The coin-cell lithium-ion battery in these applications typically has 1100-mAhr capacity, but companies working on these systems want to shrink the battery. Design goals to reduce the battery size to at least half of this level make aggressive power-management efforts even more important. A TPMS could implement as many as four stop modes, a wait mode, and a run mode to reduce power consumption and meet the 10-year target life when the average current is below 2 µA (**Figure 4**).

Because lower power consumption and optimized power management have become integral parts of system design, microcontroller designers will continue to squeeze current levels to provide very-low-power-rated products. In the future, the lowest power-consumption microcontrollers will have even lower current by reducing the contribution from digital circuitry and by using library and process modifications. In addition, reducing the voltage output of the voltage regulator and implementing new low-power run and wait modes will take power consumption to even lower levels.EDN

AUTHOR'S BIOGRAPHY

Matt Ruff is an engineer with Freescale Semiconductor's automotive-systems-engineering organization. He graduated from The University of Texas—Austin in 1997 with a bachelor's degree in electrical engineering. During college, he worked for Alcatel Network Systems in the company's interoperability labs. Ruff began his career with Motorola in February 1997, working as an applications engineer. Throughout the last eight years, he has been part of the systems-engineering team at Motorola and now carrying over to Freescale Semiconductor, specializing in automotive-multiplexing technologies, such as CAN (controller-area network), LIN (local-interconnect network), and J1850. He has helped to develop several multiplexing microcontrollers and holds a patent related to LINs. He has been a member of the Society of Automotive Engineers and a member of the SAE Vehicle Networks for Multiplex and Data Communication Standards Committee for seven years as well as a member of the SAE J2602 LIN Task Force.

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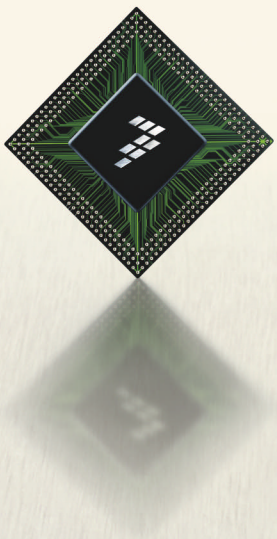

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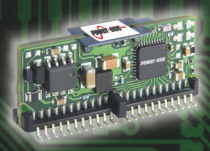

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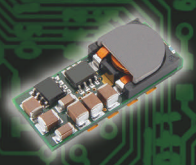

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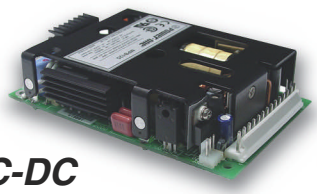

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Small, high-performance ICs require wafer-level-RF measurements

ALTHOUGH ACCURATE AND REPEATABLE RESULTS REQUIRE DIFFERENT INSTRUMENTATION AND TECHNIQUES, DON'T BE INTIMIDATED. HERE ARE THE BASICS AND SOME FINER POINTS OF WAFER-LEVEL-RF MEASUREMENTS.

Continuing increases in the speed of semiconductor devices combined with higher levels of integration, on-chip wireless functions, and the usage of mixed-signal-device designs are driving new requirements for wafer-level-RF measurement. Many device categories that system designers have thought of as purely digital now include on-chip wireless functions. Therefore, parameters such as unity-current-gain crossover frequency and maximum frequency of oscillation have become even more critical for large groups of design and test engineers. Meanwhile, the march to higher speed continues even for standard logic devices. Also, RF is becoming more necessary for isolating, measuring, and modeling some key parameters in advanced processes, especially those that use advanced dielectrics. A key advantage of wafer-level-RF measurements is the fact that making measurements at the wafer state reduces development time by eliminating the time that it takes to package a die before testing. Also, measuring the device in the prepackage state eliminates potential disturbances from the package itself. The upshot is that many engineers who once relied primarily on low-frequency or dc measurements are now adding RF to their test suites.

FROM DC TO RF CHARACTERIZATION

Engineers who are currently relying on dc characterization need to be aware of the significant changes they must make when they move to RF techniques. DC characterization measures currents or voltages using meters and sources and provides a simple response that is not phase-dependent. Occasional dc-test-instrument calibration is necessary. Service personnel often perform this calibration at regularly scheduled service intervals, so users do not give much thought to calibration issues.

RF characterization, on the other hand, measures RF phase and magnitude using S parameters (scattering parameters) and reflection ratios. The RF technique is analytically convenient and provides a complex response, and the calibration process is central to making accurate measurements. For example, unless you properly analyze and characterize reflection ratios for the test apparatus and cabling, you can't accurately extend the measurement-reference plane to a wafer device using probes and cables. RF techniques rely heavily on frequent calibration (**Figure 1**).

RF-MEASUREMENT METHODS

With RF measurement, a number of practical issues can add challenges to achieving highly accurate results. **Figure 2** illustrates the contrast between an ideal RF and the real-world environment. **Figure 2a** shows the RF stimulus. In the ideal system, the RF source stimulates the DUT (device under test). Meanwhile, the acquisition system samples the magnitude and phase of the incoming or incident signal, the reflected signal, and the transmitted signal. Of course, you must terminate the device output in impedance that matches that of the test system. In an ideal system, by looking at the phase and magnitude of the three signals—incident, reflected, and transmitted—you can easily make such measurements as gain, delay, and reflection coefficient. However, in a real-world environment, extending the measurement reference plane to a device on a wafer or substrate is challenging because, at high frequency, you can't easily define exactly where the measurement system ends and the DUT begins (**Figure 2b**).

Items such as cables, couplers, connectors, and probes combine to create a nonidealized test situation. You must even

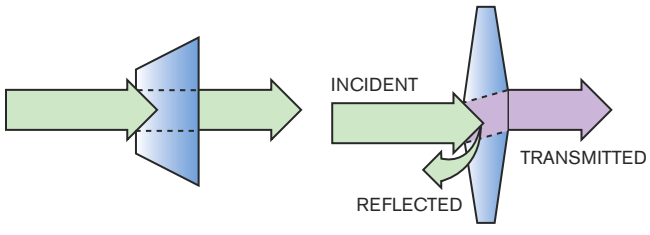

Figure 1 Compared with dc measurements (a), RF measurements are more complex because they involve the added dimension of time or phase and their accuracy and stability depend strongly on frequent calibration (b).

consider the nonideal nature of the network analyzer. You can think of the RF-measurement system—the total system with all its elements—as an RF instrument with an error-adapter network that models the system's nonideal components. Only by modeling the system's nonideal components can you correct for such errors as poor response or noisy data and assure yourself of repeatable measurements. Ultimately, the system accuracy depends on the model's accuracy.

So, although calibration is important, consistently obtaining correct data critically depends on the repeatability of the measurement system itself. Without repeatability, no amount of vector-error correction or calibration can correct for random errors, such as noise or changes in attenuation, electrical length, phase, or other environmental factors. Therefore, when you extend the measurement-reference plane to the wafer, you must use high-quality components to minimize systematic errors.

ACCURATE RF MEASUREMENT

The key system elements you need to achieve accurate and repeatable RF measurements are precision RF-wafer probes, cabling, impedance standards, and disciplined calibration and validation. RF probes provide the vital link between the test system and the DUT. Although RF-wafer probes first emerged many years ago, high-quality probes' basic characteristics haven't changed much over time. To deliver repeatable S parameters, an RF-wafer probe should exhibit a low return loss and low insertion loss, along with low—and highly repeatable—contact resistance. Low signal-to-signal crosstalk is desirable for dual-line RF probes. Also, it is important to minimize parasitic coupling at the probe tip, which can cause inaccuracy. Precision RF probes are essential for measurement of such properties as gain, return loss, and VSWR (voltage-standing-wave ratio).

Of course, the probe needs to match the DUT layout. Most RF probes have two or three contact points at the probing end—either a two-contact GS (ground-signal) probe or three-contact GSG (ground-signal-ground) probe, with some dual or specialized probes providing even more contacts.

Figure 3 illustrates some of the parasitics that come into play when you use a probe to contact a wafer device. The yellow portion of the diagram shows the probe needles, and the blue section shows the DUT. The ground in the **figure** is the back surface of the wafer. As you can see, parasitics are factors with both the on-wafer probing pads and the probe needles.

The contact-pad size can affect the parasitic values and can cause differences even when you use a calibration standard. Through proper design and by properly selecting probes, you can minimize parasitics at the probe tip. The objective is to keep parasitics small and repeatable. **Figure 4** compares some common RF-probe-tip approaches and contrasts GS pads with GSG and a microstrip configuration with shielding. **Figure 4a**

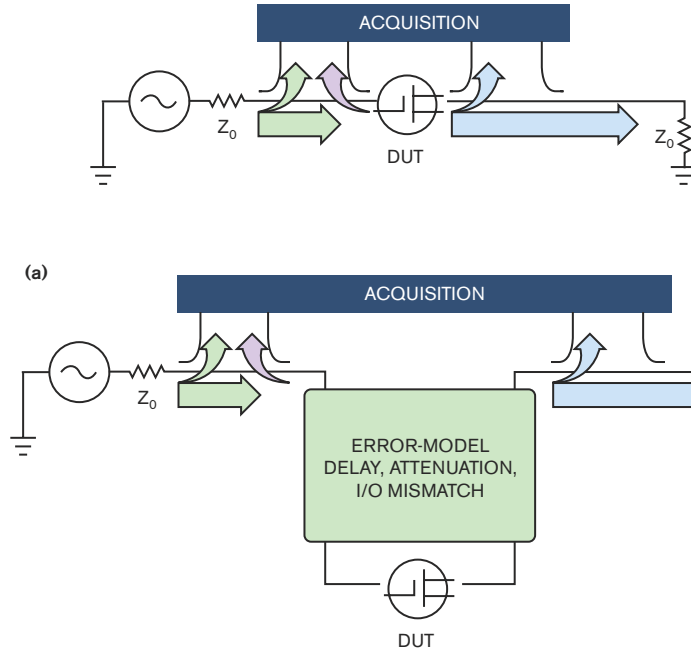

Figure 2 In ideal (a) and real-world (b) RF measurements, delay, attenuation, and impedance mismatches can produce unstable results.

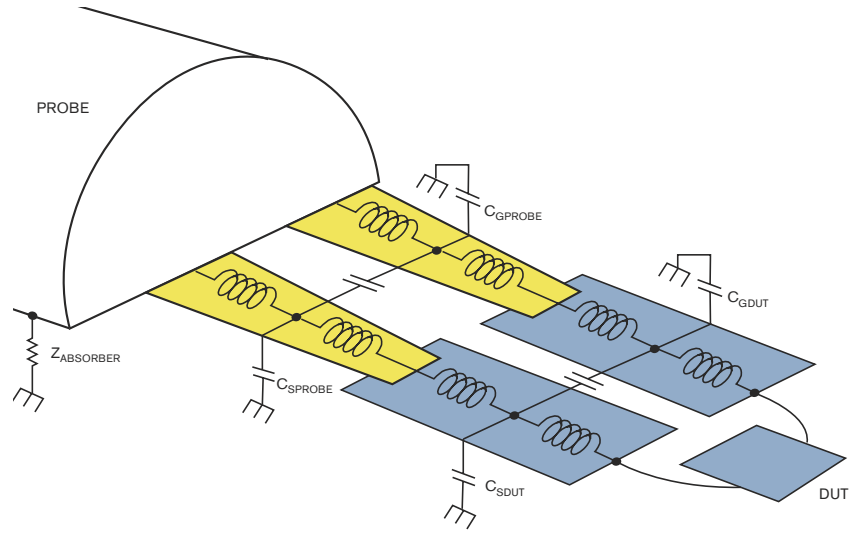

Figure 3 Although unexpected leakage resistance is occasionally a problem with certain dc measurements, you must count on having to deal with parasitic capacitance and inductance in all RF measurements.

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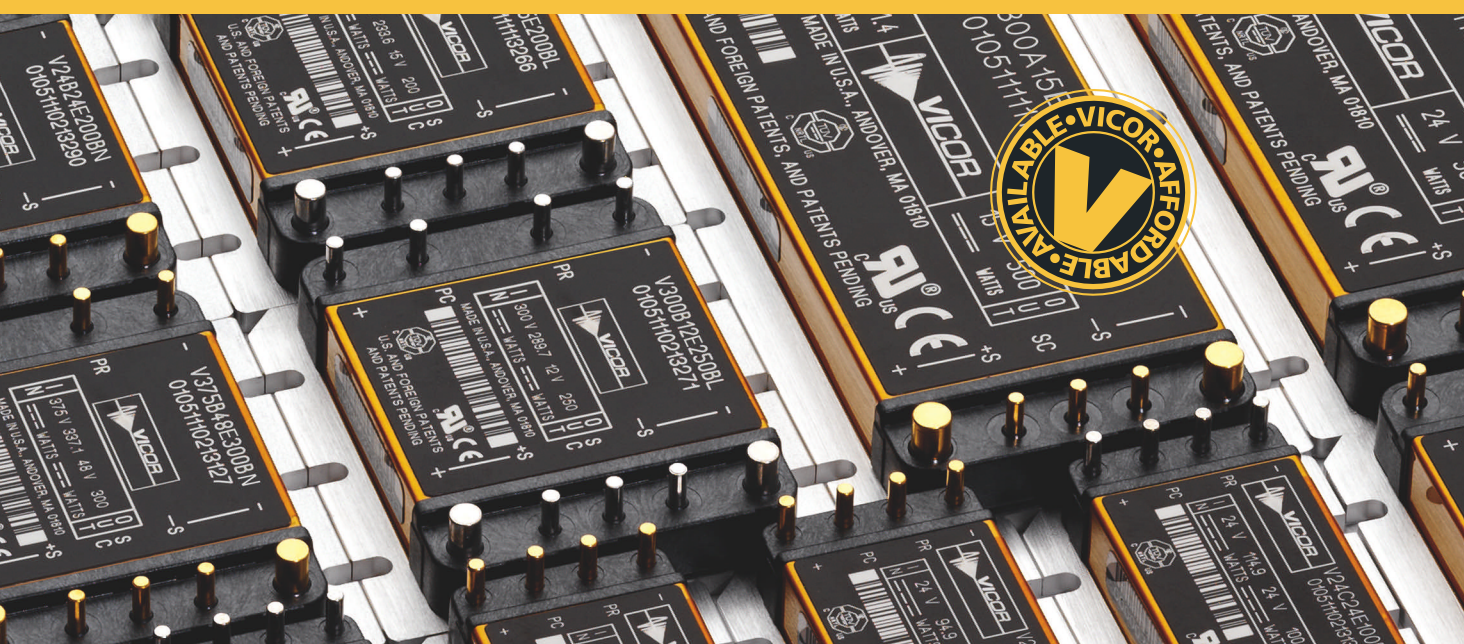


shows a two-contact GS-probe configuration with some of the fringing fields on one side coupling to the wafer or to the wafer chuck. Because of the lack of field control, you should not use GS probes for frequencies higher than 10 GHz. **Figure 4b** shows a GSG probe. As you can see, by controlling the ground path directly through the probe tip, this three-contact configuration does a much better job of terminating the field lines. Some minor interaction occurs with the DUT, but the fields on both sides of the DUT are consistent, making the three-contact approach better for higher frequencies. **Figure 4c** illustrates an advanced configuration in which the probe tip uses a microstrip line with a coplanar transition at the probe needles. Microstrip transmission lines on the probe's thin-film tips confine fringing fields more tightly than do conventional flexible coplanar tips, and the resulting improved field confinement reduces unwanted coupling to nearby devices or other probe tips, thus increasing RF-measurement accuracy. Besides preventing the field lines from interacting with the DUT, microstrip minimizes crosstalk, which makes it possible to configure dense, fine-pitch multitip probes that simultaneously handle more test points and higher frequencies.

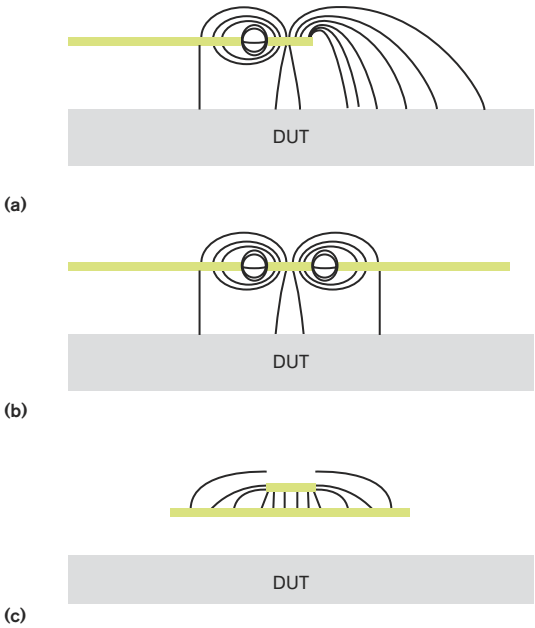


Figure 4 A GS probe is unsuitable for measurements higher than 10 GHz; GS pads fringe to the ground plane (a). A GSG-probe configuration produces more stable RF measurements than a simpler GS probe, provides better field termination, and is better for high-frequency measurements (b). The microstrip-probe configuration produces more stable measurements than either of the others (c). It shields the DUT, reducing coupling and crosstalk.

RF CABLING

Whereas much of the focus is correctly on the probe interface, you should also consider the importance of proper RF-cabling design, configuration, and quality. Although cabling represents a relatively small percentage of the overall test-system cost, in an RF-test environment, skimping on cabling or assuming that just any cable will do the job never makes sense.

Cables should provide low attenuation, high flexibility, and highly repeatable electrical recovery following flexure. In addition, they should exhibit consistent phase stability over a range of temperatures, especially because you make many RF measurements while holding the target devices at elevated temperatures. Just a few degrees of temperature change can significantly affect the electrical length of a low-quality cable. To minimize undesired effects, you must use stable, carefully specified cables and keep them clean and properly torqued. Too often, cables have been lying around the lab for years and are of unknown quality. Dirt, nicks, and excessive torque often compromise the cable connector, even though the cable material itself may be good. Some users go to great pains to use low-cost cables, taping them down so that they don't pick up vibration from movement in the room and to protect them from drafts and vibration from air-conditioning units and the like. Despite such precautions, such systems still experience

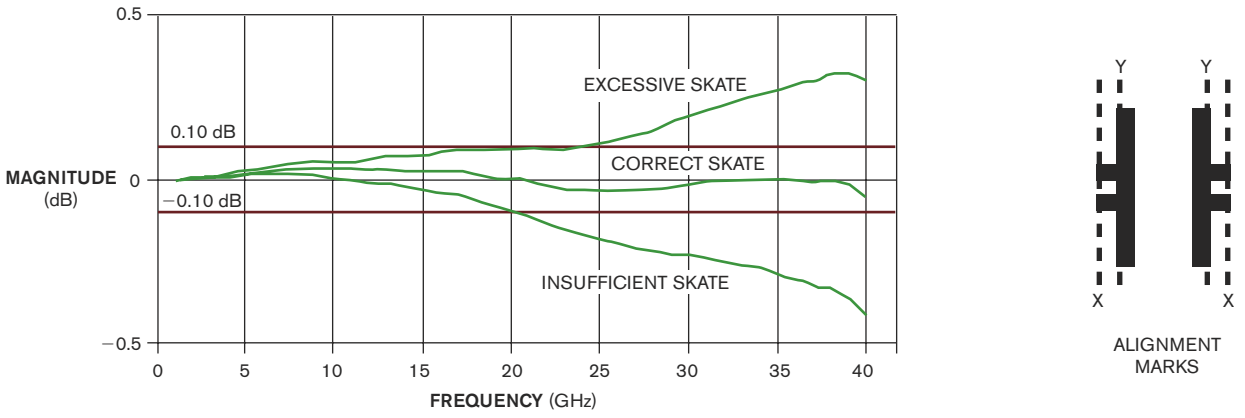
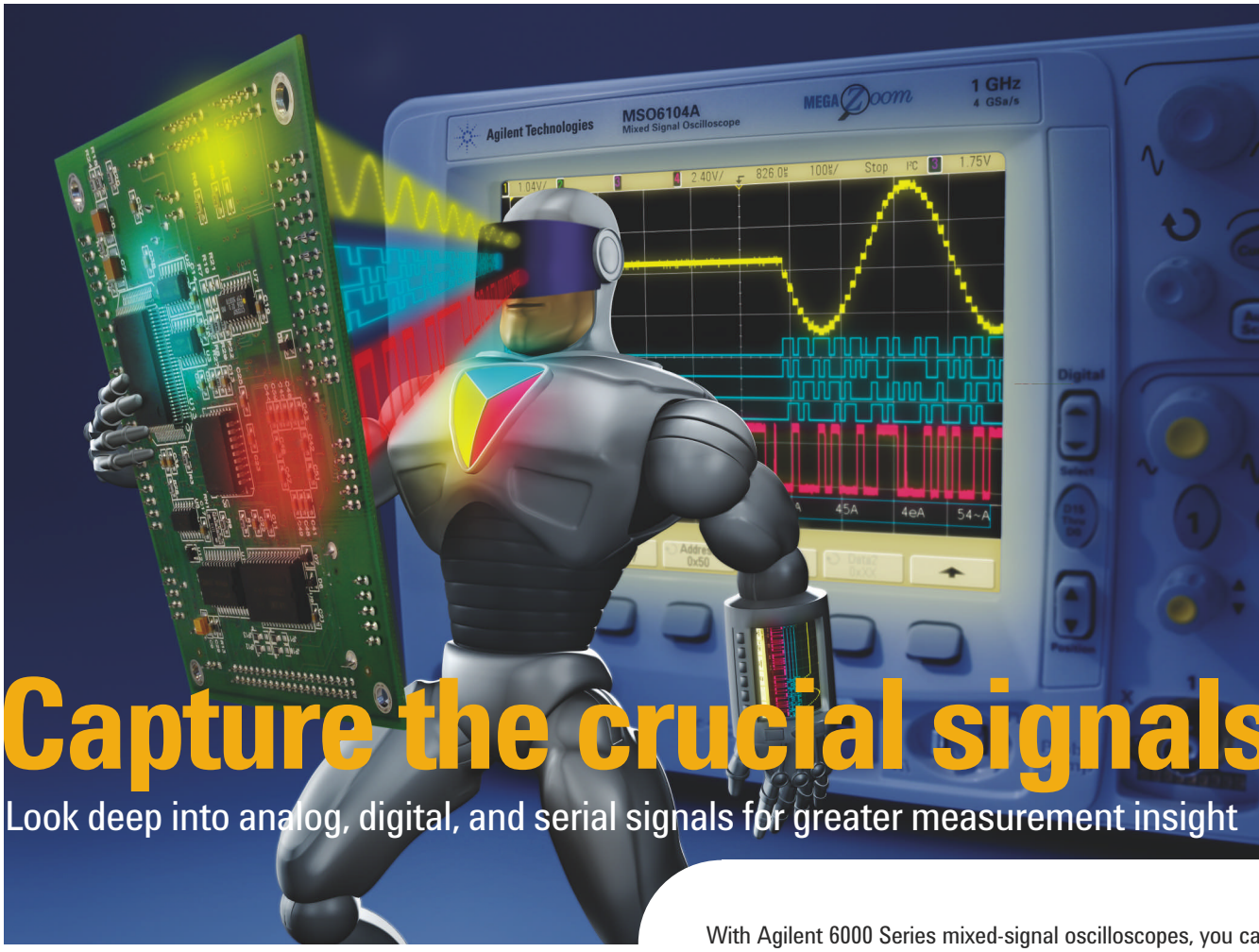


Figure 5 Probe overtravel, or skate, affects electrical measurements. Too much skate is as bad as too little. ISS alignment marks assist you in adjusting for proper probe skate.



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significant random calibration errors because, occasionally, someone bumps a cable with his elbow, and the cable can't recover quickly enough from the shock. A better approach is to invest in RF cabling that can withstand the demands of the test process and then to configure and maintain the cabling in a disciplined manner.

CALIBRATION INVOLVES CAREFUL, ACCURATE RF MEASUREMENT OF KNOWN STANDARD DEVICES OR IMPEDANCE STANDARDS.

STANDARDS

The final key element of an RF system is calibration, which is essential for highly accurate RF measurements. Calibration, or vector-error correction, involves careful, accurate RF measurement of known standard devices or impedance standards. By measuring the known standards, you can identify and remove undesired effects from subsequent measurements of the DUTs. Calibration standards typically include short, open, load, and through delay. The short is just that—with all probe tips contacting a common conductor. You typically measure the open using a probe-in-the-air method, with no connections for any of the probes. You measure load using a precision-trimmed, 50Ω load resistor. For the through delay, you use a short transmission line of known delay—usually 1 psec. Convenient off-wafer mounting of the standards is also important to allow easy integration of calibration into the measurement process—ideally, with readily available standards mounted as discrete independent substrates.

Accurate calibration requires a combination of the impedance standards themselves, an off-wafer-mounting site for the standards, and software to manage the calibration and system validation. Many people are just starting to use RF in their test suites, and, with some of the new requirements, such as multiport and differential measurements, calibration has become more challenging, complex, tedious, and error-prone. Calibration-management software addresses these issues not only by automating the entire calibration process, but also by providing guidance for system setup, tracking of system elements, and help to users in understanding the process. The wizards and tutorials that are part of comprehensive calibration software can speed learning, more quickly get users up and running, and help with optimization of measurement sequences. For example, software can remember and track all of the probe dependencies for various calibration values, such as which electrical values apply to a particular probe. This information ensures that calibration errors can't occur simply because an operator enters a wrong value when setting up a system. If undetected, such a simple error can propagate a long string of incorrect values and incorrect calibrations, resulting in numerous incorrect measure-

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ments over an extended period. As with cabling, an investment in calibration software can greatly enhance the value of the entire RF system.

Many customers use only an open transmission line or open stub for calibration validation. In measuring an open stub, you can look at the reflection coefficient on the Smith chart. With increasing frequency, it should show an inward spiral and roll-off. If it's a good match and good calibration, the open stub should also show a linear-phase-transmission response.

WAFER-LEVEL ERRORS

Three of the most common errors that affect wafer-level RF measurement are incorrect probe planarization, dirty connectors on cables or probes, and improper probe placement on standards. Planarization is the process of using the adjustment on the probe arm to make sure that all of the probe tips make contact with the device in a parallel plane. For example, with a GSG probe, it is critical that all probes come in uniform contact and have equal scrub areas on the DUT pads. One of the tools for making planarization easier, a contact substrate, provides a check area for making probe contact and examining the contact scrub marks. You can then make probe-planarity adjustments to ensure a good contact. If possible, you should use systems with dual off-wafer-mounting sites for both a contact substrate and an impedance-standard substrate. You should also provide proper cable-strain relief to make sure that the cables don't pull the probes out of planarity. In addition, calibration software is useful in that it offers optimization tools that make it possible to electrically determine the consistency and integrity of probe contacts.

GET IN THE HABIT OF ALWAYS CHECKING FOR PROPERLY CLEANED PROBE NEEDLES TO PROVIDE ELECTRICAL STABILITY AND LOW CONTACT RESISTANCE.

The second frequently encountered error condition relates to material accumulation on cable connectors or probes. A simple discipline such as occasionally cleaning and swabbing the cable connectors with isopropyl alcohol can make a world of difference, as can regularly checking the connector fit with a torque wrench. The probe needles themselves also can pick up debris over time, especially when probing on aluminum. Get in the habit of always checking for properly cleaned probe needles to provide electrical stability and low contact resistance.

Visually inspect probe tips and first clean them with air. For standard needles, you can also use a soft brush, isopropyl alcohol, or both. Remember to brush away from the body of the probe. For some more advanced probes, such as those based on thin-film technology,

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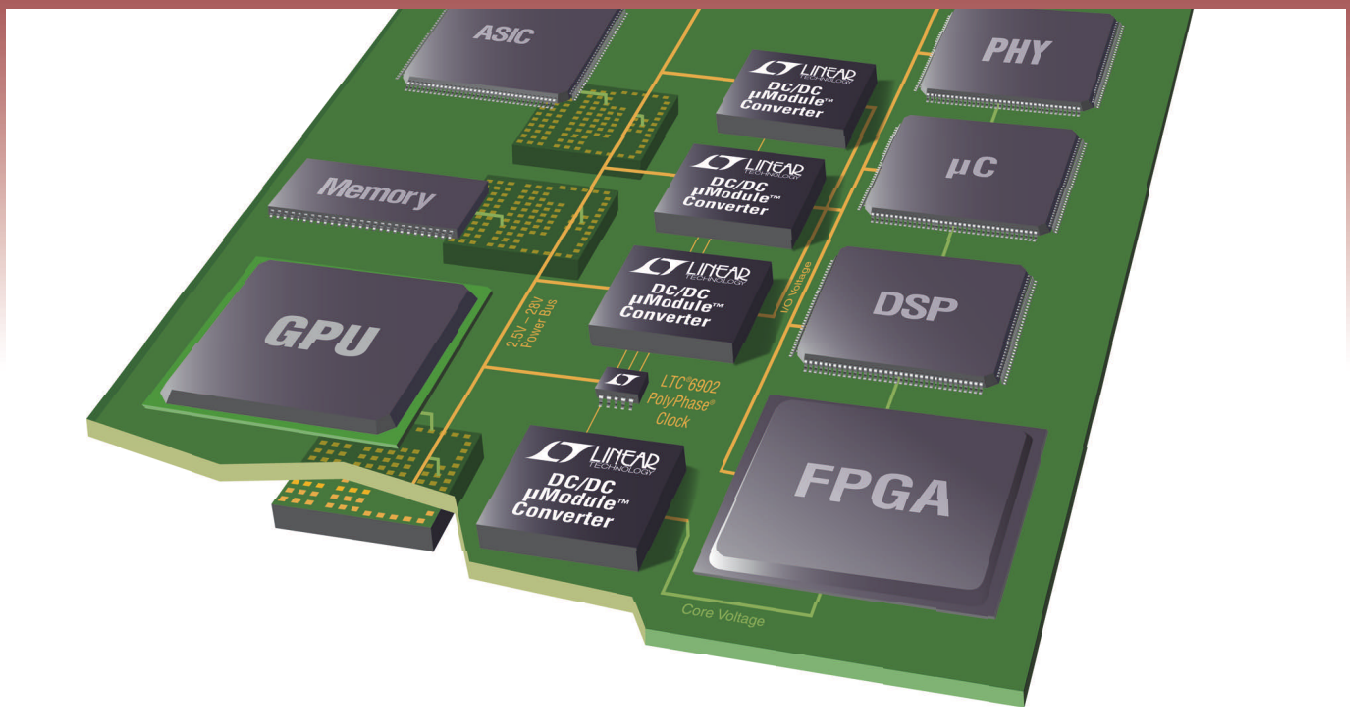

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µModule DC/DC Converters for Core, I/O, Clock & System Power

V_{IN}: 4.5V-28V; V_{OUT}: 0.6V-5V						LGA Package (15°C/W)	
Part No.	I_{OUT} (A)	Current Share	PLL	Track, Margin	Remote Sense	Height (mm)	Area (mm)
LTM®4602	6	Combine two for 12A to 24A or 4x LTM4601 for ≤48A				2.8	15x15
LTM4603	6		✔	✔	✔		
LTM4603-1	6		✔	✔			
LTM4600	10						
LTM4601	12		✔	✔	✔		
LTM4601-1	12		✔	✔			
V_{IN}: 2.25V-5.5V; V_{OUT}: 0.8V-3.3V							
LTM4604*	4	2x for 8A	✔			2.3	9x15

*Future Product

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Application Notes
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it's more appropriate to use semisticky materials, such as a gel pack, which can cleanly attach itself to the debris and pull it off the probe tip.

Another common error is improper probe overtravel, or skate, especially when contacting impedance standards. "Skate" is the distance that the probe moves across a device or standard when you apply a downward force to make contact. The degree of skate electrically affects the measurement, whether it is on the DUT or on a calibration standard. Both excessive and insufficient skate can significantly affect the results by changing the inductance of the contact interface (**Figure 5**). To help control this effect, calibration-standard substrates typically incorporate alignment marks that allow users to adjust the amount of scrub to control overtravel and maintain electrical stability. Once again, proper use of software helps. By using software to automate the calibration, you can get consistent probe placement—not just on the scrub, but also in controlling x, y, and z placement. Research has repeatedly proved that calibrations under automatic software control are more repeatable than those using manual probe placement.

As devices scale down and add functions, it is clear that the need for RF-measurement techniques is increasing. Also, the development of new differential, multiport devices has driven a movement to RF disciplines. In addition, new differential, multiport devices and balanced measurements rely on RF probes with better crosstalk performance and for better software to prevent errors due to increased calibration complexity.

Although you need to prepare for a future that includes RF measurements, the good news is that the necessary tools and processes have for years been in place and undergoing refinement. The most important factors are understanding the key differences between RF and lower frequency measurements; making wise investment in a high-quality wafer-level test system; and developing solid disciplines for system setup, calibration, and maintenance. EDN

AUTHOR'S BIOGRAPHY

Larry Dangremond is product manager for RF systems at Cascade Microtech (Beaverton, OR), where he has worked for 13 years. He manages the company's high-frequency-probing product line and is responsible for product road maps, life-cycle management, and Cascade's presence in RF segments. He holds a bachelor's degree from Portland State University (Portland, OR). Outside work, he most enjoys outdoor activities, including bicycling, hiking, fishing, and golfing.

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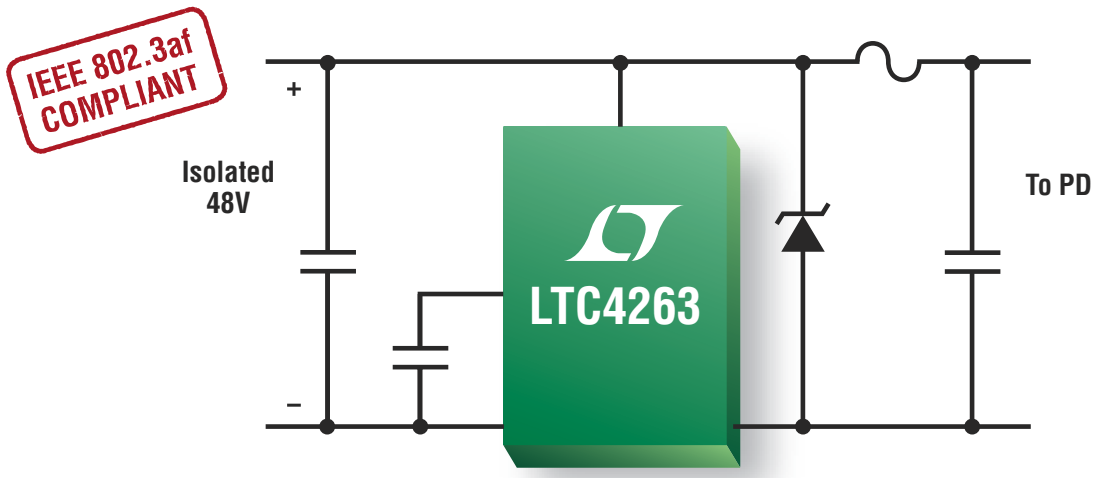
Single Port PoE



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- Powered Device (PD) Detection and Classification
- LTC4263: $2.95 each in 1k qty

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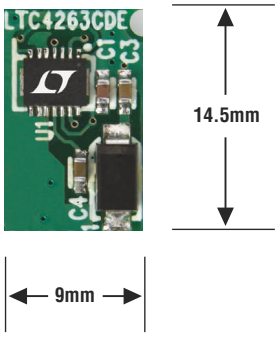

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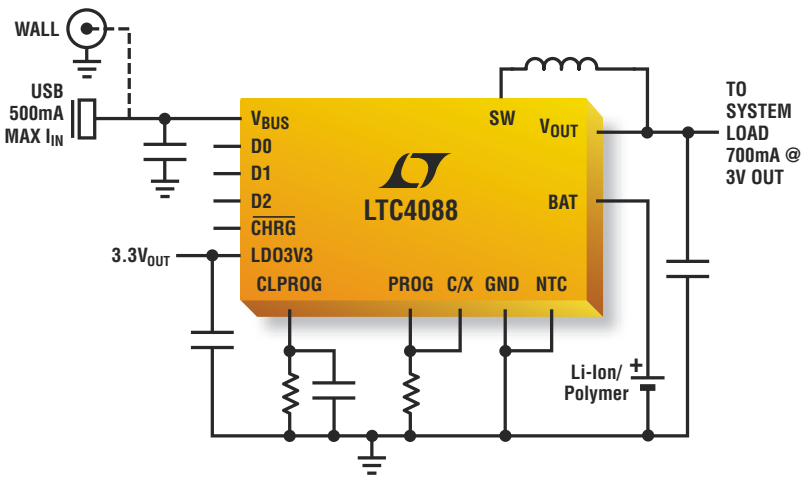

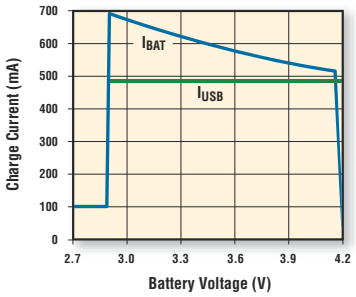

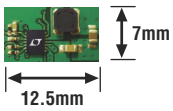

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LTC®4088	Switching	4.35 to 5.5V (7V max)	Timer with C/x Indication	3mm x 4mm DFN-14	Bat-Track™, Programmable Input I_{LIM} Maximizes Available Power from USB Port
LTC4066	Linear	4.35 to 5.5V (7V max)	Timer with C/x Indication	4mm x 4mm QFN-24	Integrated 50mΩ Low Loss Ideal Diode
LTC4085	Linear	4.35 to 5.5V (7V max)	Timer with C/10 Indication	3mm x 4mm DFN-14	Integrated 200mΩ Low Loss Ideal Diode (<50mΩ Capable Option)
LTC4089	Linear	4.35 to 36V (40V max)	Timer with C/10 Indication	3mm x 6mm DFN-22	Bat-Track, "Instant-ON" Operation, High Voltage Input Switching, with Current Limiting from USB
LTC4067	Linear	4.25 to 5.5V (13V OVP)	Timer with C/10 Indication	3mm x 4mm DFN-12	Up to 1.25A Charge Current, Integrated 200mΩ Low Loss Ideal Diode
LTC4090	Linear	4.35 to 36V (60V max)	Timer with C/10 Indication	3mm x 6mm DFN-22	Bat-Track, "Instant-ON" Operation, High Voltage Input Switching, with Current Limiting from USB

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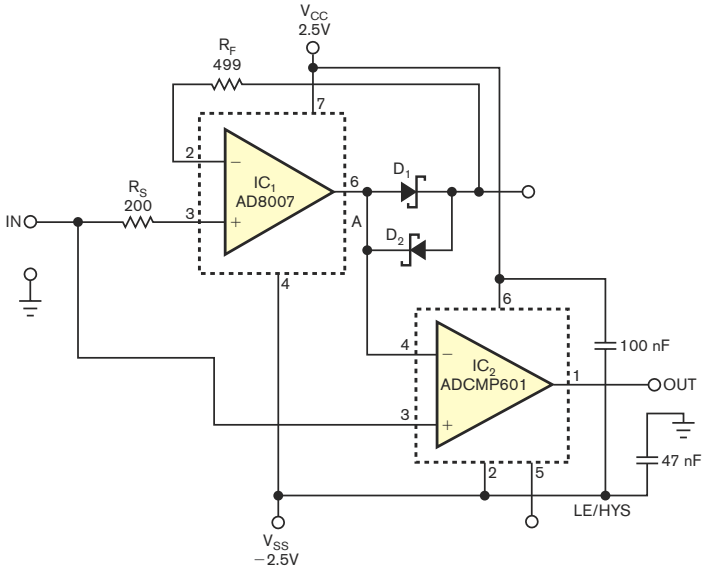
Comparator detects position of peaks and valleys in a waveform

Marián Štofka, Slovak University of Technology, Bratislava, Slovakia

The recent advent of Analog Devices' (www.analog.com) ADCMP60x family of comparators has filled a gap between the less-than-1-nsec-response comparators consuming 100 to 200 mW and those exhibiting approximately 1-µsec response, requiring about one-thousandth that power. The ADCMP60x comparators exhibit a low value of the product of propagation-delay-by-supply-current drain; possess rail-to-rail input and output operation; and offer a variety of options for hysteresis, latch-mode operation, and shutdown mode. Some of them also have inherent level-translating capability. Moreover, the ratio of propagation delays for the positive and negative transitions at the output is close to the ideal value of 1 within 8% tolerance for the ADCMP600, ADCMP601, ADCMP602, and ADCMP603 and with in a 6.7% tolerance for the ADCMP608 and ADCMP609 members of the family (**Reference 1**).

This ratio is important in applications in which both positive- and negative-output-level transitions are equally significant. **Figure 1** shows one such circuit. Voltage-level transitions at the output of the detector indicate changing of the sign of the first derivative of the input signal; in other words, the circuit detects time positions of peaks and valleys in the input-voltage waveform. The detector circuit uses an ADCMP601 for IC_2, and IC_1 is an Analog Devices AD8007 current-feedback amplifier. IC_1 connects as a voltage follower with an antiparallel combination of Schottky-barrier switching diodes, D_1 and D_2, between the output and the inverting input of the amplifier. Comparator IC_2's inputs connect to the source of the input voltage and to the output of the current-feedback amplifier. This configuration enhances the voltage difference of $V_{IN}-V_A$ between inputs of the comparator. It performs this enhancement in a steplike manner at the instant, or region, at which the sign of slope of the input signal changes. This voltage difference is a measure of the double-forward voltage of diodes D_1 and D_2 at their forward current, which you derive from V_{IN}/R_F.

You use a current-feedback amplifier as IC_1 because a dynamic current flows into its inverting input even when you



NOTE: D_1 AND D_2 ARE HSMS-282Ls OR HSMS-282Cs.

Figure 1 Comparator IC_2 produces an output that switches state at the positive and the negative peaks of the input-voltage waveform.

DIs Inside

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connect it as a voltage follower. The values of the R_S and R_F resistors are those that **Reference 2** recommends for a gain of 1. You needn't worry about instability due to the presence of antiparallel diodes in the feedback path of the current-feedback amplifier. These diodes increase the value of feedback resistance to more than 499Ω. Whenever the input voltage is only approximately 0V, the frequency-gain response of IC_1 for an R_F value greater than 499Ω remains flat.

An analysis of the response of the voltage follower in **Figure 1** to a harmonic input voltage uses ω/ω_T and $\omega=2\pi f$, where f is the input-voltage frequency and ω_T is the radial transition frequency of the amplifier. At the radial-transition frequency, the ratio of Z_M (the magnitude of the amplifier's transimpedance) to R_F drops to one. This simplification leads to an **equation** for the delay, t_D, in **Figure 2**:

$$\Delta\varphi = 2\sqrt{\frac{V_F}{V_m}\times\frac{R_F}{r_{m0}}},$$

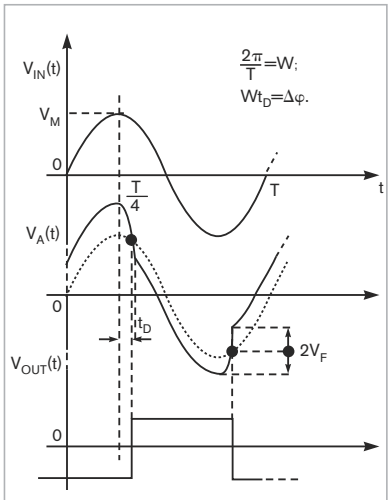

Figure 2 The output of comparator IC_2 switches a slight time delay, t_D, after the positive and the negative peaks of the input voltage.

where V_F is the forward voltage of diode D_1, V_m is the amplitude of input voltage, R_{m0} is the dc transresistance of the current-feedback amplifier, and Δϕ is the electrical-error angle in radians. The period of input harmonic voltage, T in **Figure 2**, represents 2π radians. The final error of the detector is Δϕ, which decreases by a factor of $\sqrt{2}$. This reduction occurs because the necessary operating overdrive over the midpoint of the steplike transition in the $V_A(t)$ voltage that the comparator requires is more than an order of magnitude less than the value of V_F.EDN

REFERENCES

1 "Rail-to-Rail, Very Fast, 2.5V to 5.5V, Single-Supply TTL/CMOS Comparators," ADCMP600/ADCMP601/ADCMP602 Preliminary Data Sheet, Analog Devices, March 2006, www.analog.com/UploadedFiles/Data_Sheets/378991928ADCMP600_1_2_prra.pdf.

2 "Ultralow Distortion High Speed Amplifiers," AD8007/8008 Data Sheet, Analog Devices, 2003, www.analog.com/UploadedFiles/Data_Sheets/AD8007_8008.pdf.

Precision integrator sparks current-ratio-to-frequency converter

Stefano Salvatori and Gennaro Conte,
Università degli Studi di Roma Tre, Rome, Italy

The Design Idea in **Figure 1** uses the S_1 switch of the Texas Instruments (www.ti.com) IVC102 precision integrator to select between a single input current or the superposition of two input currents. This function allows you to obtain an output signal whose characteristics directly relate to the ratio between the two input currents. The circuit achieves high accuracy independent of most of the system parameters. In addition, you can enhance accuracy if you let a digital counter control the IVC102-based circuit (**Figure 2**). In this case, the system's output is a number in the BCD (binary-coded-decimal) format proportional to the input-current ratio, realizing a true digital conversion.

The circuit divides into two phases. The first phase begins when the output voltage of the IVC102 becomes slightly greater than the threshold voltage of the LM311 comparator. The comparator generates a falling-edge signal, and the 555 monostable starts a pulse, which closes S_1. In this case, the total input current, I_2-I_1, generates a negative-going ramp if I_2 is greater than I_1. In the delta-time period, ΔT_A, the integrator's output voltage reaches the final voltage value. Hence, $|V_{FIN}-V_{TH}|=(I_2-I_1)\Delta T_A/C_{INT}$, where C_{INT} is the value of the IVC102's integrating capacitor. When the 555 monostable's output pulse ends, the second phase starts: S_1 opens, and input current I_1 discharges C_{INT}. The ΔT_B for the output voltage to assume the threshold voltage's value is then $C_{INT}|V_{FIN}-V_{TH}|/I_1$, and the comparator generates a new trigger command to the monostable so that a new cycle can start. Manipulating the previous **equations** yields: $I_1/I_2=\Delta T_A f$, where $f=(\Delta T_A+\Delta T_B)^{-1}$. This **equation** states that the generated output signal, a train of pulses, has a frequency, f, proportional to the I_1/I_2 current ratio. The accuracy of the monostable directly affects the accuracy of the system. Conversely, the integrating capacitor's and threshold voltage's values do not influence the accuracy if they maintain constant values at least in the 1/f time scale.

You can increase the accuracy of the circuit in **Figure 1** by modifying the section that generates the constant, ΔT_A-wide pulse. The circuit in **Figure 2** generates a ΔT_A-wide pulse using three

(continued on pg 108)

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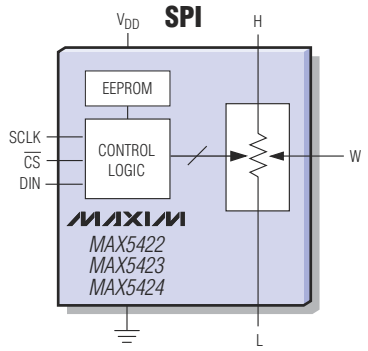

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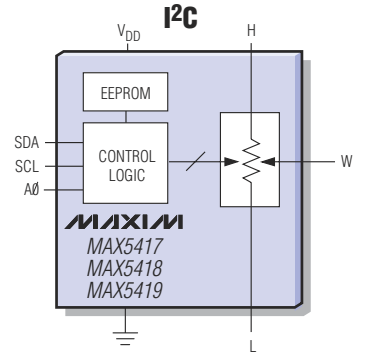

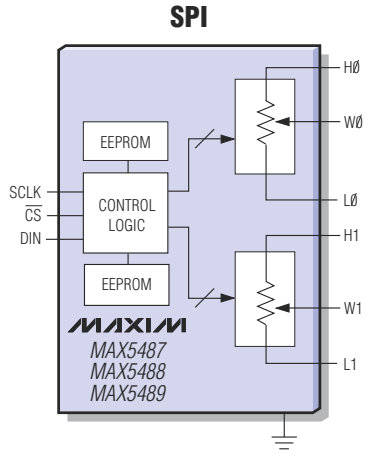

Dual

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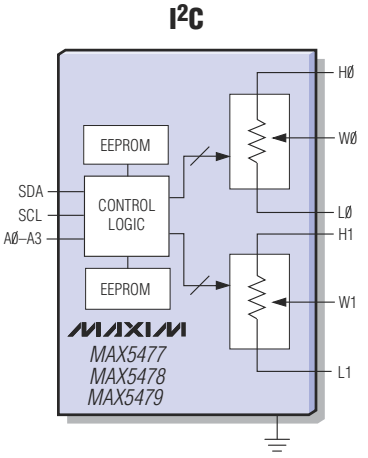
- Single 2.7V to 5.25V Supply
- 1µA (max) Standby Supply Current
- 8 Unique I²C Addresses Per Product



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MAX5487/MAX5488/MAX5489	2	SPI	10/50/100	1.60

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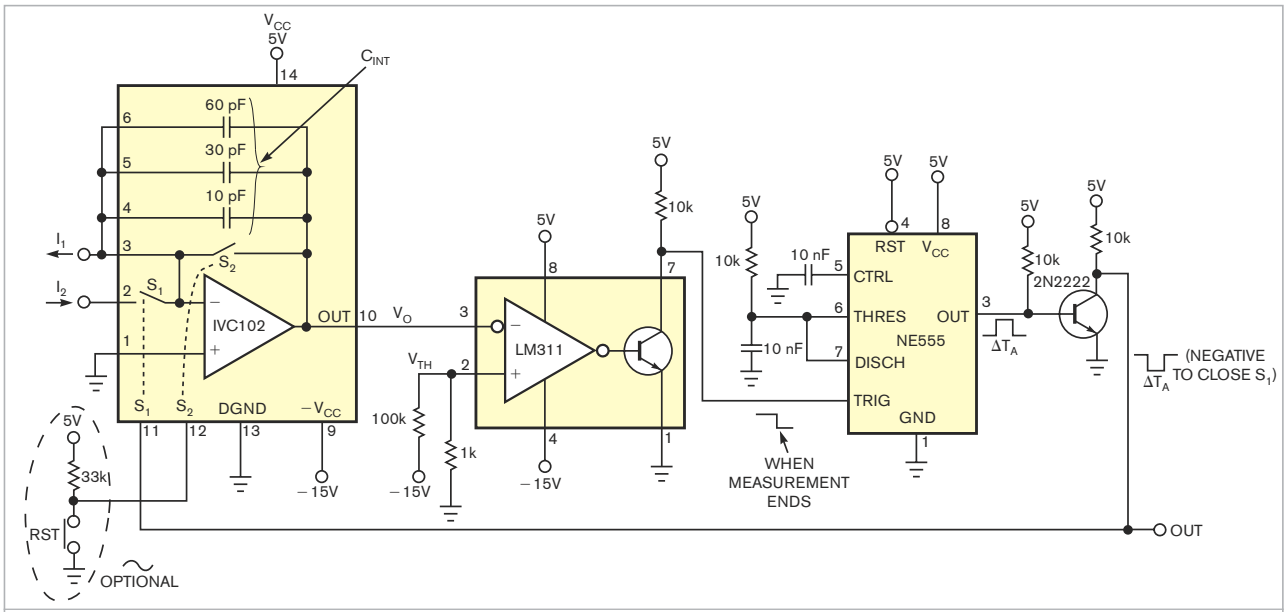

Figure 1 This circuit allows you to obtain an output-signal frequency that directly relates to the ratio between the two input currents.

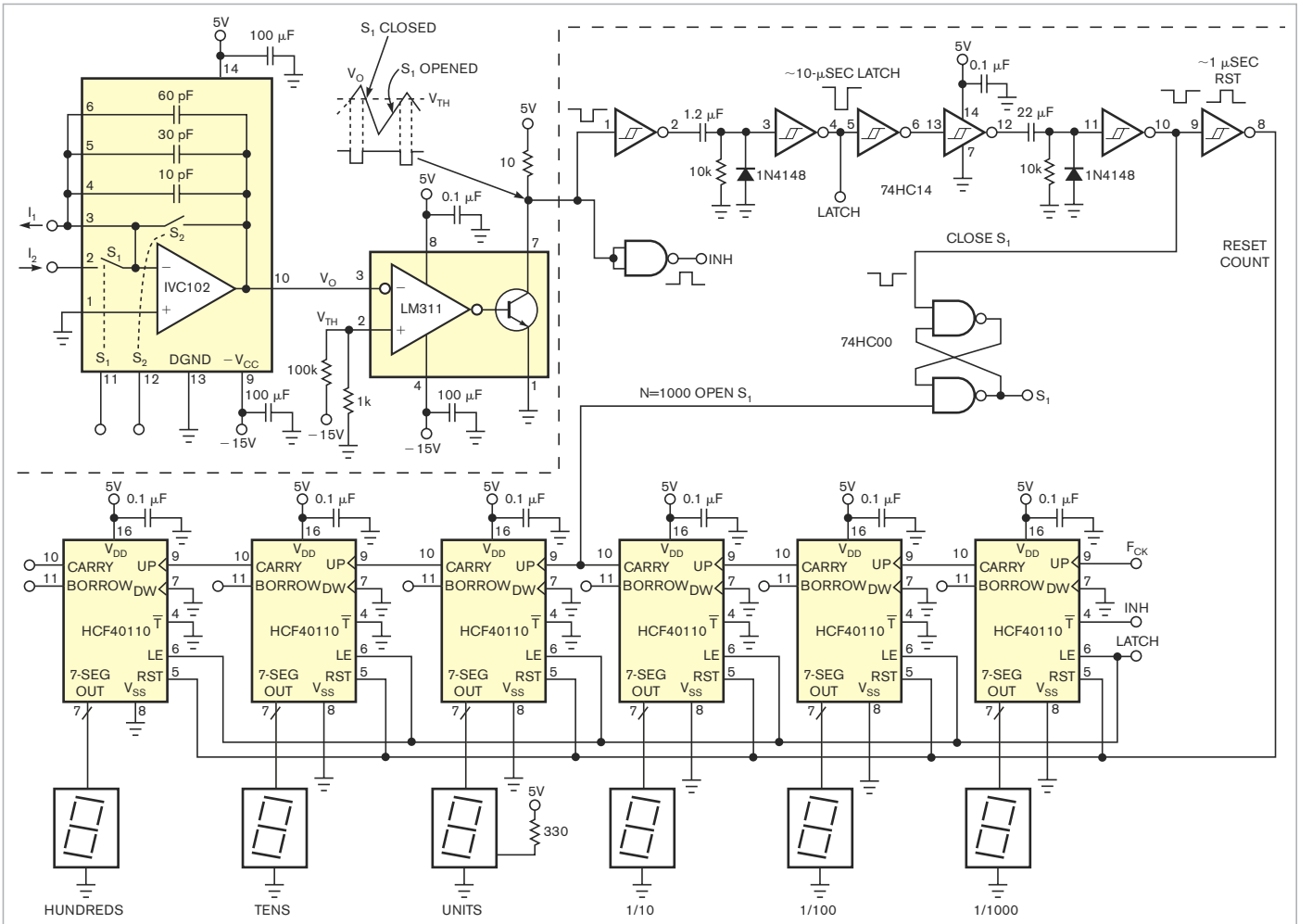

Figure 2 To the circuit in Figure 1, this design adds a BCD counter to obtain direct readouts on seven-segment LED displays.

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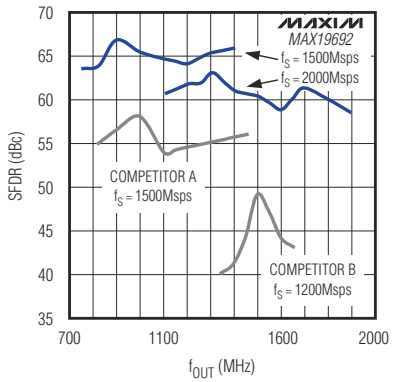

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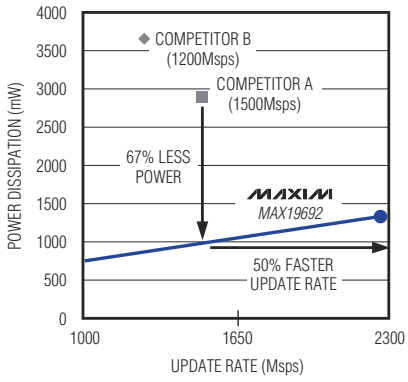

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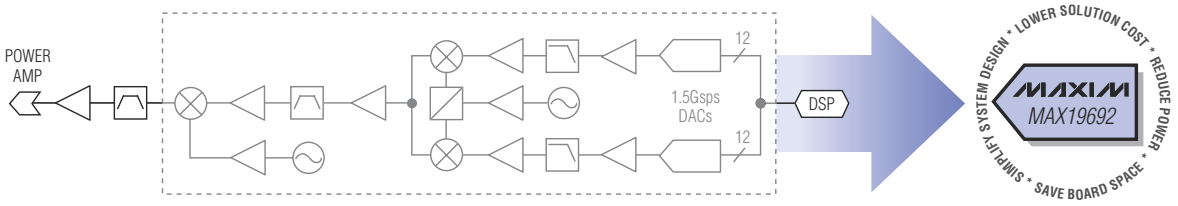

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(continued from pg 104)

HCF40110 BCD counters. When the third counter generates a carry, 1000/f_{CK} seconds have elapsed. In **Figure 2**, a set/reset flip-flop controls S_1's state, and the 74HC14 hex inverter with a Schmitt-trigger input generates the pulses that reinitialize the system. A brief description of the measurement cycle follows. When the IVC102's output voltage becomes greater than the threshold voltage, the INH (inhibit) signal connected to the toggle input of the first HCF40110 inhibits counting. At the same time, the negative-going edge of the comparator output generates a negative-going pulse of approximately 10 µsec, which latches the counters' values at the output to display the actual result. After this step, a negative-going pulse sets the SR flip-flop to close S_1. A corresponding positive-going pulse resets the counters. The latch-enable lines of the 40110s are tied high, so the counters' reset doesn't affect the displayed value. When the reset pulse ends and the comparator's output goes high, the HCF40110s can count up. When the third counter generates a carry (negative-going pulse), the 1000th clock period has elapsed, and the SR flip-flop resets to open S_1. The cycle ends at the next falling edge of the comparator's output. The time period in which $I_2 - I_1$ charges C_{INT} is $N_A/f_{CK}(N_A=1000)$, and the I_1 requires for discharging is N_B/f_{CK}. Manipulating the integrator-related relationships yields $I_2/I_1=N/N_A$, where $N=N_A+N_B$.EDN

Accurate USB 2.0 temperature sensor needs only a handful of parts

Silvio Lauckner, Ismaning, Germany

This Design Idea presents a simple, accurate, and reliable design to measure temperature using the USB. **Figure 1** shows the complete circuit of the temperature-sensor device. The heart of the sensor device is an FT232RQ USB-to-serial converter from FTDI (Future Technology Devices International, www.ftdichip.com). In addition to using the FT232 in its default UART mode, the FT232 works in a so-called bit-bang mode (**references 1**, **2**, and **3**). This mode changes its I/O lines into a bidirectional data bus, which the user can fully control. The connection with the USB takes place in a standard manner, and the back end of the chip interconnects to an AD7814 digital temperature sensor from Analog Devices (www.analog.com, **Reference 4**).

The temperature sensor uses a four-wire SPI but only three pins: SCK (serial clock), SS# (slave select), and SDO (serial-data out). To avoid any malfunction of the sensor, the SDI (serial-data-in) line must be grounded. The FT232 acts as an SPI master and emulates the protocol for the AD7814 by setting or clearing the appropriate port pins for SS# and SCK. The data from the sensor gets read back together with all the other bus lines. This process occurs simultaneously with the write process.

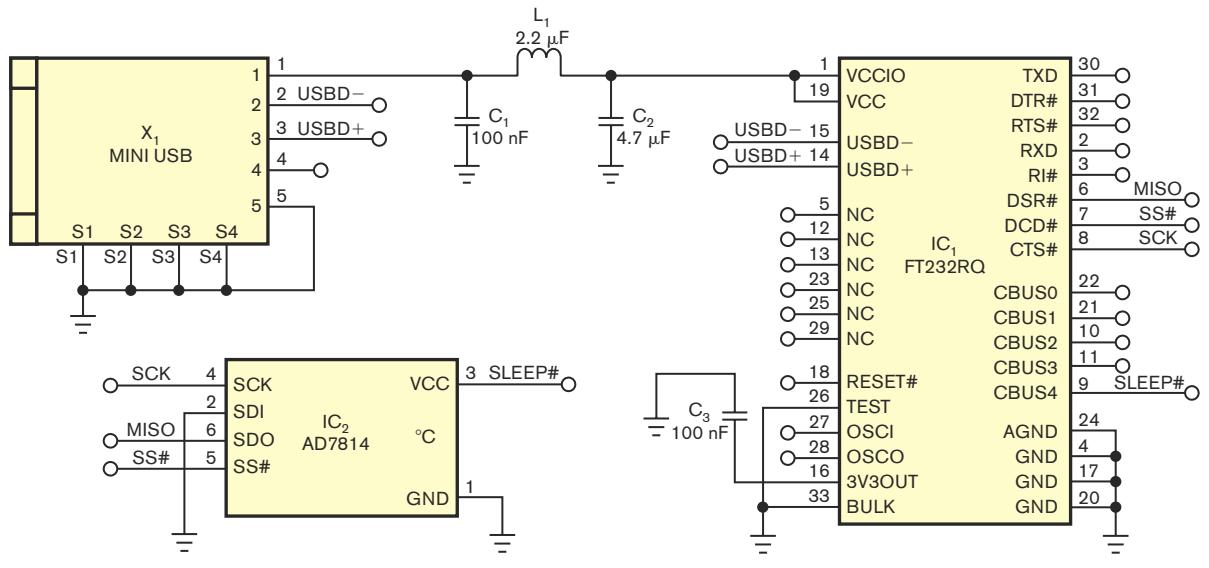

Figure 1 This circuit for a USB temperature sensor works in default UART and bit-bang modes.

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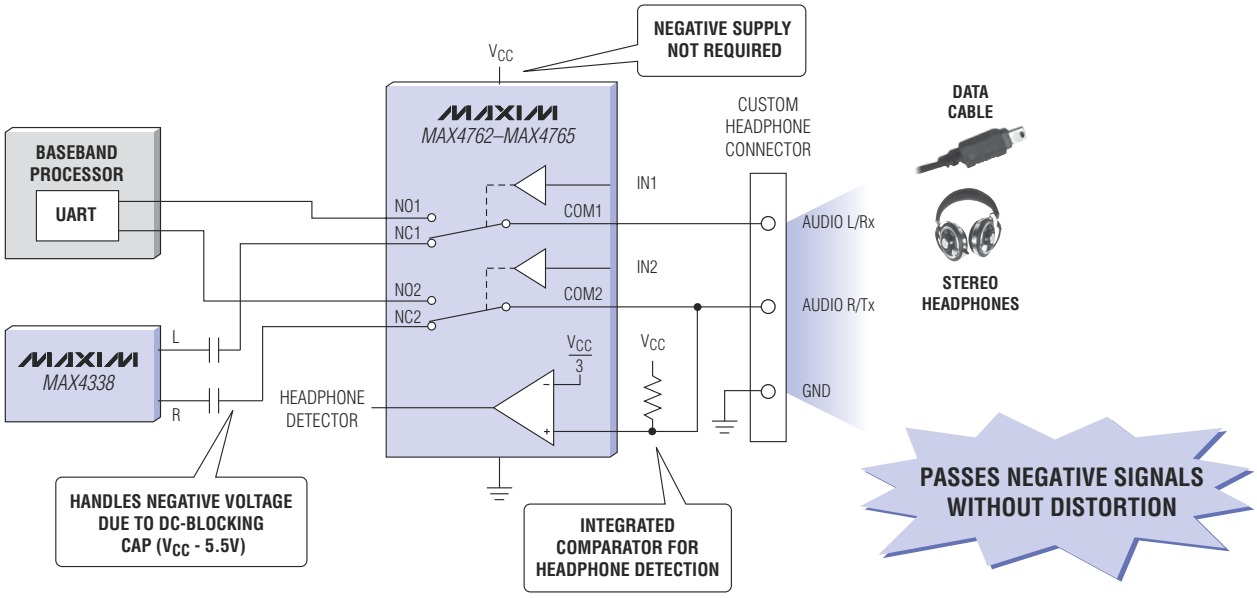
0.4Ω Switches Have Integrated Comparator in a Tiny Chip-Scale Package



Excellent Linearity and Low Distortion

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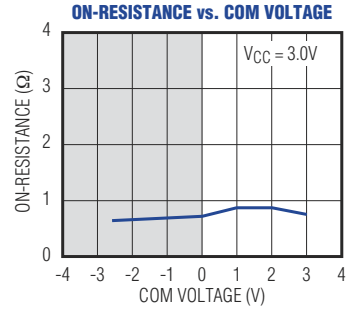
- 0.3Ω R_{ON} Flatness
- 0.03% THD+N
- Clickless Switching



Part	Function	R_{ON} (Ω)	R_{ON} Flatness (Ω, max)	Comparator	Shunt Switch	Supply Voltage (V)	Package
MAX4762	Dual SPDT	0.4	0.3	No	No	+1.8 to +5.5	10-µMAX®/TDFN/12-UCSP™
MAX4763	Dual SPDT	0.4	0.3	Yes	No	+1.8 to +5.5	12-UCSP/QFN
MAX4764	Dual SPDT	0.4	0.3	No	Yes	+1.8 to +5.5	10-µMAX/TDFN/12-UCSP
MAX4765	Dual SPDT	0.4	0.3	Yes	Yes	+1.8 to +5.5	12-UCSP/QFN

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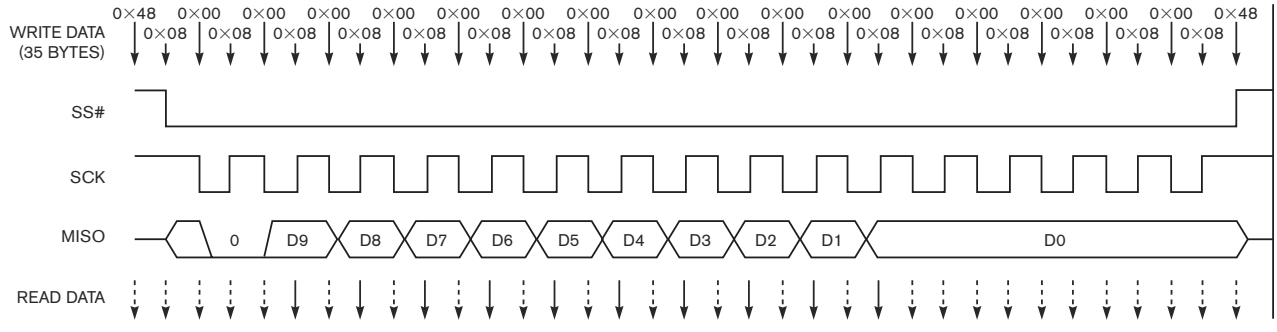

Figure 2 The timing diagram for the AD7814 shows considerable data overhead to download 10 bits of temperature data.

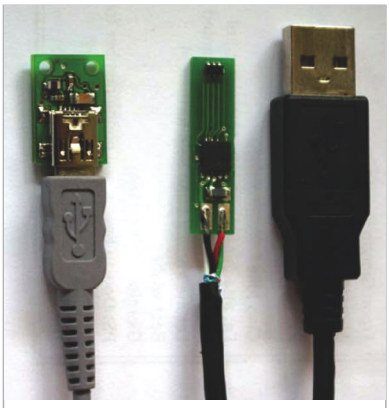

Figure 3 Two sample circuits (left and center) are smaller than a USB Type A plug (right).

To comply with the USB specification, you power down the temperature sensor using the sleep signal while the USB logic is in suspend mode. The sensor device receives its power through the USB and draws only about 20 mA. On the software side, you need only to open the device and switch the chip into the bit-bang mode. After that action, you can send the fixed pattern to emulate an SPI master from the host PC to the FT232 (**Figure 2**). The software returns a data array of the port samples of both the PC and the FT232, whose ports are inputs and outputs.

Because the FT232 chips come with a unique serial number, you can identify the correct device within a multichip environment. So, you can put more than one FT232-based sensor onto a computer. The core of this Design Idea is not limited to measuring temperature. You can use other sensors with digital interfaces, as well.

To get the current temperature, you must write 35 fixed bytes into the port register. The sensor expects 16 clock pulses on the SCK line while the SS# is low. The clock frequency is 1 MHz. The device samples sensor-read data during the write operation. After the protocol on the back end finishes, you can retrieve the data from the host PC for further processing. To get just 10 bits out of the sensor involves considerable data overhead (**Figure 2**). The dashed-line arrows mark the bytes, which need no further evaluation.

This Design Idea realized two sample circuits on a two-layer PCB (printed-circuit board) measuring only 18×12 mm (0.7×0.47 in.) and 7.6×30.5 mm (0.3×1.2 in.). **Figure 3** shows them in comparison to the size of a USB Type A plug. EDN

REFERENCES

1. "FT232R USB UART IC," Future Technology Devices International, 2005, www.ftdichip.com/Documents/DataSheets/DS_FT232R.pdf.
2. "AN232R-01 Bit Bang Modes for the FT232R and FT245R," Future Technology Devices International, 2005, www.ftdichip.com/Documents/AppNotes/AN232R-01_FT232RBitBangModes.pdf.
3. "D2XX Programmer's Guide," Future Technology Devices International, 2005, www.ftdichip.com/Documents/ProgramGuides/D2XXPG33.pdf.
4. Analog Devices, Data sheets AD7814 (www.analog.com/en/prod/0,,764_814_AD7814,00.html), ADT7301 (www.analog.com/UploadedFiles/Data_Sheets/ADT7301.pdf), and ADT7302 (www.analog.com/en/prod/0,,764_811_ADT7302,00.html).

Integrator enables simple ohmmeter with gigohm range

Stefano Salvatori and Gennaro Conte,
Università degli Studi di Roma Tre, Rome, Italy

The Texas Instruments (www.ti.com) IVC102 precision integrator has high-quality internal capacitors. The circuit in **Figure 1** allows you to measure very-high-resistance values of R_X. A precision difference amplifier, a TI INA105, applies a reference voltage to R_X. During integration, a negative voltage ramp, V_O, is generated at the output of the IVC102. The two LM311s compare the amplitude of V_O with two fixed thresholds and generate the two digital signals: start and stop. The delta time between two such events relates to the system parameters by the expression: $\Delta T = C_{INT}[(V_A - V_B)/V_{REF}]R_X$, where ΔT is the delta time and C_{INT} is the internal integrating ca-

LINEAR TECHNOLOGY

DESIGN NOTES

Drive Large TFT-LCD Displays with a Space-Saving Triple-Output Regulator – Design Note 417

Jesus Rosales

Introduction

The power appetite of large TFT-LCDs appears to be insatiable. Power supplies must feed increasing numbers of transistors and improved display resolutions, and do so without taking much space.

The triple output supply shown in Figure 1 shows a compact design based on the LT3489, which is optimized for driving large TFT panel displays. The main output provides 8V at 600mA while the 23V and –8V outputs provide 10mA and 20mA respectively, all from a 3.3V input. Even though TFT converters generally run from a regulated 3.3V or 5V source, this converter can operate seamlessly from a Lithium-Ion battery, delivering 5W when the battery is drained to 3.3V and 8W when it is at 4.2V.

The LT3489 squeezes a 2.5A, 0.12Ω, 40V switch into a tiny 3mm × 3mm MS8E footprint. It offers external or internal compensation, an internal soft-start, a 2MHz switching frequency, and it is also pin compatible with the popular LT1946. The design process with the LT3489 is easy and predictable.

The circuit in Figure 2 operates as a SEPIC converter, allowing the output to be higher or lower than the input. Pulling the $\overline{SHDN}$ pin to ground sets the output at 0V even while the voltage source is connected to the input.

Both applications take full advantage of the soft-start feature in which a single capacitor programs the voltage ramp rate of the output at startup. The 2MHz switching frequency makes possible the use of small surface mount inductors and ceramic capacitors, which reduce the total footprint of the design. Figure 3 shows how small the triple-output TFT circuit in Figure 1 can be.

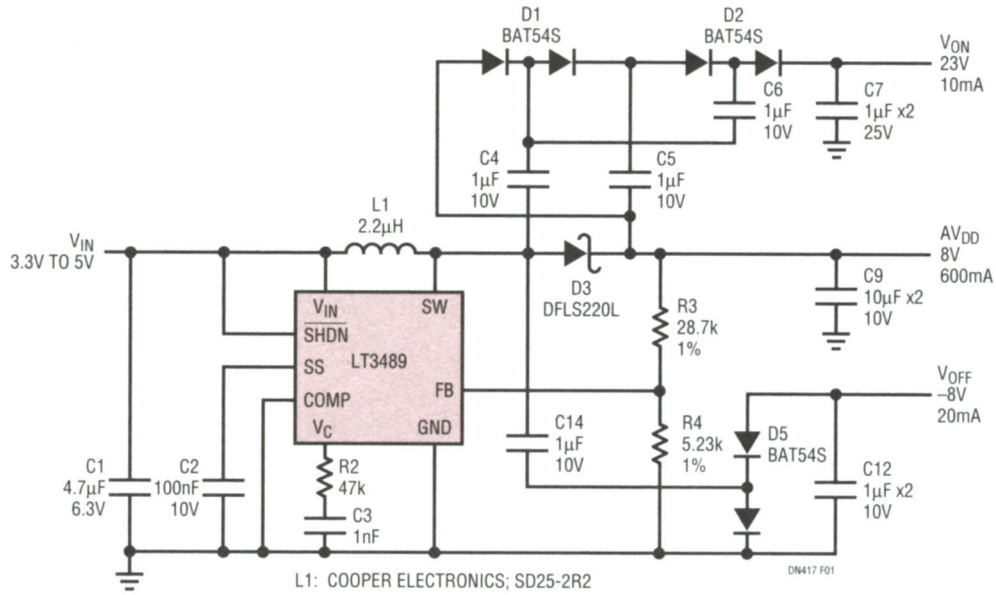

Figure 1. A 3.3V Input, Triple-Output—8V, 23V and –8V—2MHz, TFT Converter

Conclusion

For large TFT-LCD panel displays, local bias supplies, DSL modems or portable devices, the LT3489 delivers big power from a small 3mm × 3mm MS8E package. Its rugged 2.5A, 0.12Ω, 40V internal switch, soft-start feature, fixed frequency and flexible compensation simplify the design and improve the performance of many applications.

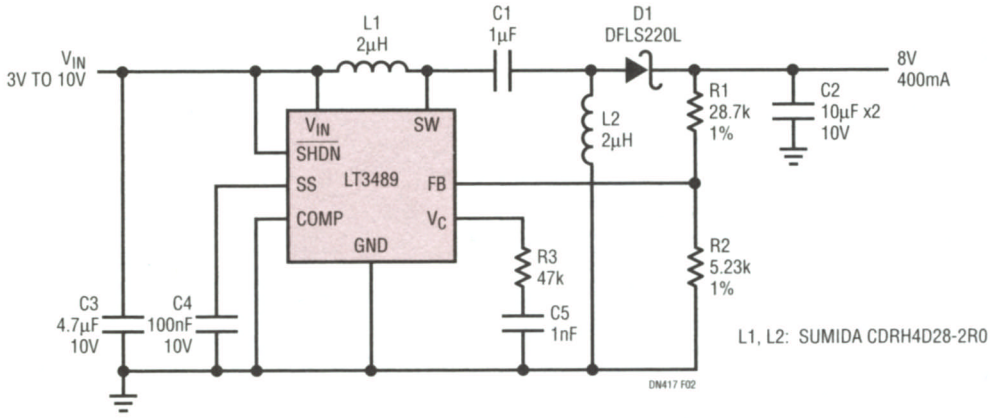

Figure 2. A 2MHz, 3V to 10V Input to 8V at 400mA to 900mA with Output Disconnect Converter

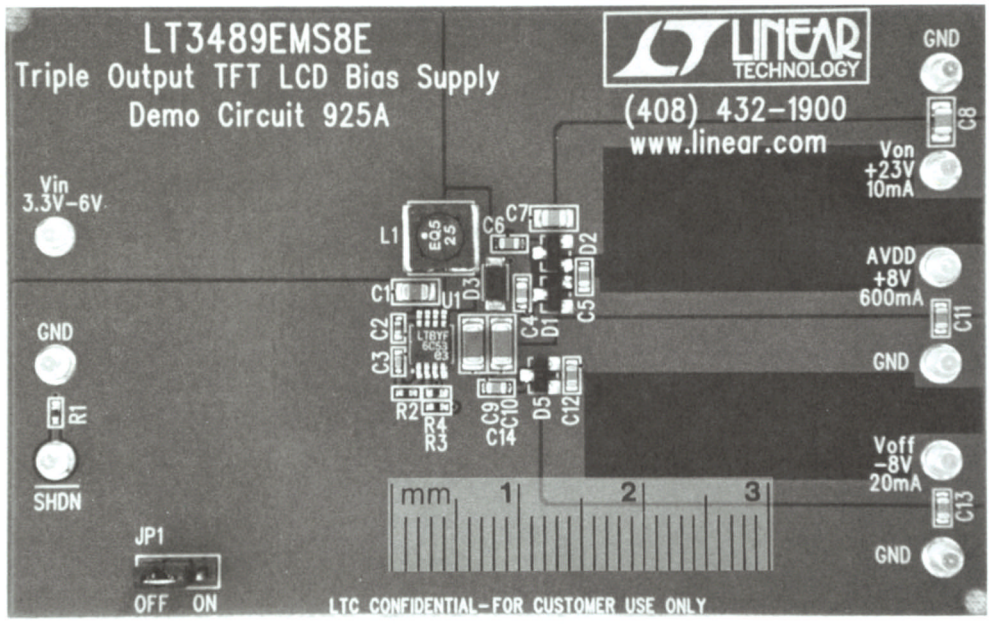

Figure 3. LT3489 Demo Circuit with Layout for the Figure 1 Schematic

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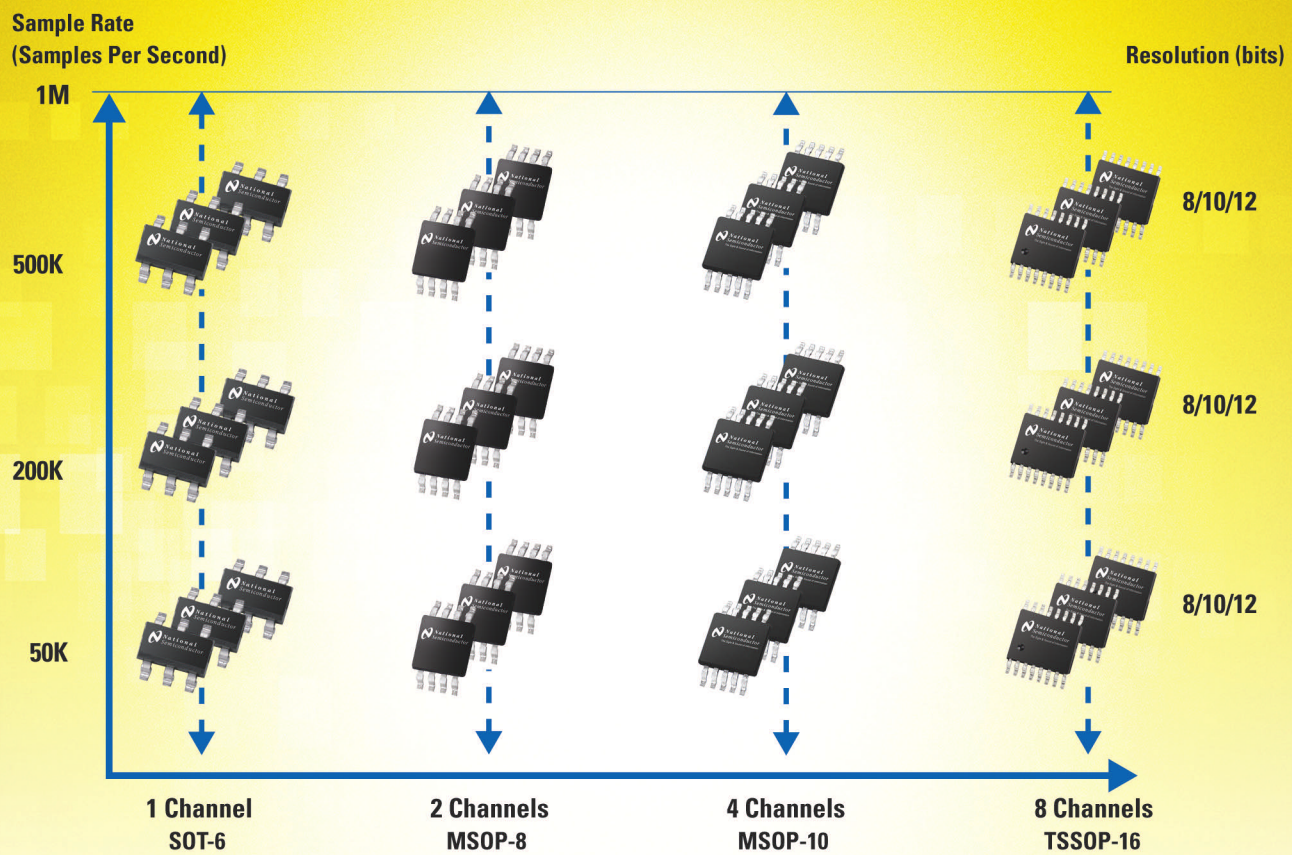

Single-Channel A/D Converter Features (Power Down: 2.5 µW)

12-Bit ADC
- INL: ±0.4 LSB
- ENOB: 11.7

10-Bit ADC
- INL: ±0.2 LSB
- ENOB: 9.8

8-Bit ADC
- INL: ±0.5 LSB
- ENOB: 7.8

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pacitance of the IVC102, which external connections on pins 4, 5, and 6 select. (Note: when S_1 is open, C_{INT}=10 pF, whereas, when S_1 is closed, C_{INT}=100 pF.) The V_A threshold allows the circuit to see the output ramp without any offset on the V_O signal. Because of the INA105 difference amplifier, $V_{REF}=V_A-V_B$, so the previous **equation** reduces to: $\Delta T=C_{INT}R_X$. Also note that the precision of resistors R_1, R_2, and R_3 is not critical. The difference amplifier guarantees the precision of the ohmmeter.

External digital-control circuitry can measure delta time by counting the clock periods between the start and the stop events. At the end, the control circuit can generate a reset signal for the IVC102 to perform a new measurement. EDN

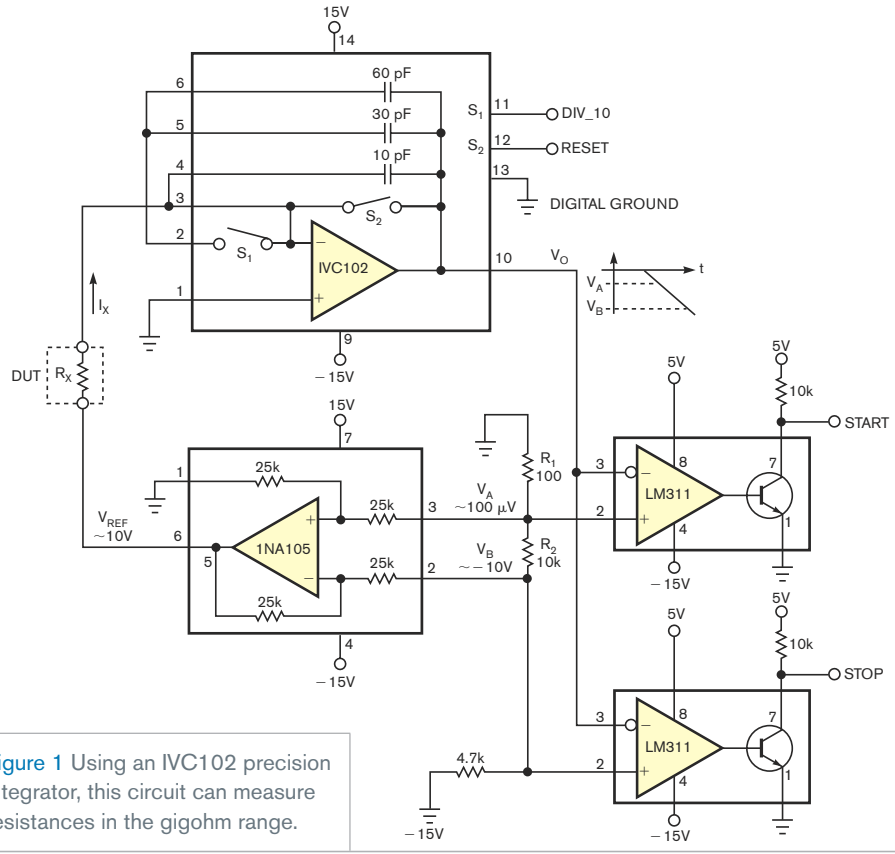

Figure 1 Using an IVC102 precision integrator, this circuit can measure resistances in the gigohm range.

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productroundup

POWER SOURCES

Quarter-brick, dc/dc-power modules claim 92% typical efficiency

Available in a quarter-brick format, the PKM4515ZE PI, PKM4619E PI, PKM-4810E PI dc/dc modules provide a 48V input voltage. The PKM4515ZE PI runs at 24V at 2.1A and provides a 50W output, the PKM4619E PI runs at 2.5V at 25A and provides a 62.5W output, and the PKM4810E PI runs at 3.3V at 25A and provides an 80.5W output. Typically operating at 92%, the devices run at a 3.3V output voltage at half-load and operate at a 36 to 75V-dc input-voltage range. Providing 1.5 million hours MTBF at 40°C, the PKM4515ZE PI costs $21.46, and the PKM4619E PI and PKM4810E PI cost $24.68.

Ericsson Power Modules, www.ericsson.com

Photovoltaic and wind converters use two MPPT channels

The Aurora PVI-6000 photovoltaic and wind-inverter series uses two high-speed, independent MPPT (maximum-power-point-tracking) channels to allow energy harvesting in installations with multiple photovoltaic arrays pointing in different directions. Available energy increases in the grid-tie devices by using transformerless designs, providing a 97% conversion efficiency. Features include a laptop-free configuration using front-panel-mounted buttons, true sine-wave outputs with self-selecting voltage capabilities, and less than 3.5% typical total harmonic distortion. Providing grid-connected operation certified to international standards, the Aurora PVI-6000 series costs $5500.

Power-One, www.power-one.com

Midpower converters provide ZCS/ZVS

Joining the vendor's 24V-dc-input family, these nine midpower Mini dc/dc converters feature low-noise ZCS/ZVS (zero-current switching/zero-voltage switching). The devices come in a 100W model with a 3.3V output volt-

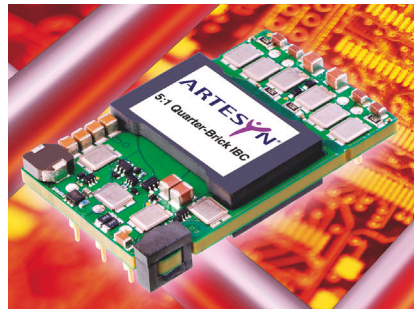
age; a 150W model with 5, 12, 15, 24, 28, 36, and 48V output voltages; and a 200W model with a 36V output voltage. Operating from a 24V nominal output, the converters have an 18 to 36V input range. Measuring 2.28×2.2×0.5 in., the Mini dc/dc converters cost $87.

Vicor Corp, www.vicorpower.com

Single- and dual-output dc/dc converters have UL approval

Available in 24 models operating from 5, 12, and 24V-dc inputs, the D200E dc/dc-converter series provides single and dual outputs at 5, 9, 12, 15, ±5, ±9, ±12, and ±15V dc. Features include a 1000V-dc I/O isolation, 87% efficiency, and low-noise operation. The UL-approved, 2W devices have a 3.5 million-hour MTBF. Available in a 0.77×0.28×0.4-in. SIP, the D200E family costs $3.60.

MicroPower Direct, www.micropowerdirect.com



Eighth- and quarter-brick IBCs feature a driven-synchronous system

Operating from a 38 to 55V-dc power supply, the eighth-brick IBC32 and the quarter-brick IBC60 IBCs (intermediate-bus converters) suit multiple downstream, nonisolated POL (point-of-load) converters in distributed-power systems with 9.6V intermediate-bus architectures. The 300W eighth-brick and 642W quarter-brick devices have a fixed 5-to-1 conversion ratio and generate an isolated, unregulated dc output. A 48V-dc power supply allows the converters to generate a 9.6V-dc output. The IBC60 delivers 60A, providing a 400W/in.^{3} power density, and a 2.5% typical load-regulation figure for all load conditions; the IBC32 provides a 32A output capacity and a 2.3% typical load-regulation figure. A synchronous-driven system allows the PWM controller to control all of the power switches, providing tighter timing control of the secondary-side switches than that of a self-driven synchronous rectifier. The eighth-brick IBC32 costs $45, and the quarter-brick IBC60 costs $60.

Emerson Network Power, www.emersonnetworkpower.com

productroundup

MICROPROCESSORS

IDE supports Windows Vista operating system

Supporting computers running Microsoft's Vista operating system, the PSoC Designer IDE (integrated development environment) 4.4 features user modules for the vendor's CapSense capacitive sensing, SD cards, and USB UARTs. The PSoC Express visual-embedded-design tool allows designers to create designs and transfer them to PSoC Designer. Available at the Software-and-Drivers section of the vendor's Web site, the PSoC Designer is free for downloading.

Cypress Semiconductor, www.cypress.com

16-bit-microcontroller family comes in 22- and 44-pin packages

Adding eight microcontrollers to the vendor's PIC24FJ64GA004 family, these 16-bit microcontrollers include the peripheral-pin-select pin-mapping function, allowing designers to map the devices to the desired pin and allowing use of all onboard peripherals. Providing 16 to 64 kbytes of flash program memory and as much as 8 kbytes of RAM, the microcontrollers are compatible with the vendor's other 16-bit families. Features include the free MPlab IDE (integrated development environment) with a Visual Device Initializer component, which graphically assists designers in mapping pins and initializing code for the peripheral-pin-select function; the MPlab C30 C compiler; the MPlab Real Ice tool; and the MPlab ICD (in-circuit-debugging) 2 tool for emulation and debugging. Additional features include two independent I^2C channels, a UART, and SPI communications. The devices cost $1.69 (10,000) and come in TQFP-44 and QFN-44 packages for the PIC24FJ64GA004, PIC24FJ48GA004, PIC24FJ32GA004, and PIC24FJ16GA004 microcontrollers, and in SOIC-28, QFN-28, SSOP-28, and SDIP-28 packages for the PIC24FJ64GA002, PIC24FJ48GA002, and PIC24FJ32GA002 models. A version of Explorer 16 is available with a 44-pin PIC24FJ64GA004 onboard for $129.99.

Microchip Technology, www.microchip.com

Decoders target HD-DVD players and Blu-ray-disc players

The vendor's HiFi 2 audio engine meets the approval of the Dolby, Dolby Digital Plus 7.1-channel decoder, Dolby Digital Plus 5.1-channel decoder/converter, and Diamond standards. Targeting use in Xtensa processors, the 7.1-channel device supports the simultaneous decoding of primary and secondary audio channels as well as simultaneous streams of 7.1-channel content on a single HiFi 2 audio engine; the 5.1-channel device converts native Dolby Digital Plus signals to 5.1-channel Dolby Digital. Targeting HD-DVD players, Blu-ray-disc players, and set-top boxes, the decoders cost $27,500 for a project license.

Tensilica, www.tensilica.com

Configurable SOCs come in dual- and single-core variants

Adding to the vendor's SPEAr configurable SOC (system-on-chip) IC family, the dual-core SPEAr Plus600 and the single-core SPEAr Head600 chip feature 90-nm-process technology. The devices integrate one or two advanced ARM926 processor cores with 16 kbytes of data and 16 kbytes of instructional cache memory, running at 333-MHz and 600,000 gates of embedded configurable logic. Additional features include 136 kbytes of SRAM, 32 kbytes of ROM, and a mem-

ory interface supporting DDR/DDR2 memories and a large connectivity-IP (intellectual-property) portfolio. The memory interface has DDR2-666-memory compatibility, allowing the same pins to drive DDR or DDR2 memory. The connectivity IP includes an IrDA interface supporting fast IrDA, Gigabit Ethernet MAC (media-access control), one device USB 2.0 port, and two host-device ports. An XGA LCD controller supports 1024×768-pixel resolution in 24-bit true color and a JPEG codec. A dithered PLL with programmable frequencies, jitter, and LVDS I/O operates at 600-MHz for high-speed-communication links. Available with dedicated development boards, the SPEAr Plus600 and SPEAr Head600 cost $10 and $12 (20,000), respectively.

STMicroelectronics, www.st.com

Evaluation platform combines microcontroller and graphical software/GUI

The 16-bit H8 microcontroller-based evaluation platform combines the vendor's H8S/2378 microcontroller and Segger Microcontroller Systems' graphical-software/GUI (graphical-user-interface) package. The device features an LCD direct-drive capability supporting QVGA-size TFT (thin-film-transistor) and STN (supertwisted-nematic) LCD panels. The demo evaluation board supports full-screen animations at 25 frames/sec on a QVGA-size panel. Available in a 20×20-mm LQFP-144 package, the H8S/2378 processor costs $8.

Renesas Technology America, www.renesas.com

Embedded USB controllers come with a USB software stack

Expanding on the vendor's ColdFire USB line, the MCF5521x microcontroller full-speed USB OTG (On-The-Go) family and the MCF5253 embedded processor with High-Speed USB OTG use the ColdFire V2 core. The MCF5521x features 128 kbytes of flash memory, 16 kbytes of SRAM, 56 general-purpose I/Os, and a two-channel periodic-interrupt timer. The device also features two I²C-bus-interface modules, four-channel 32-bit timers with DMA support, a 12-bit ADC, and three on-chip UARTs. The MCF5253 embedded processor features 8 kbytes of instruction cache, an SDRAM controller, two CAN 2.0B modules, an I²S interface, and three UARTs with flow control. In addition, the device provides a dedicated ATA hard-disk interface; a flash-media-card interface; a four-channel DMA controller with four

productroundup

MICROPROCESSORS

DMA channels; and a six-channel, 12-bit ADC. A Special Edition version of the vendor's CodeWarrior Development Studio for ColdFire version 6.4 or later supports the USB controllers. The devices also come with a complimentary USB software stack that the vendor created jointly with CMS Systems, and the vendor offers a µClinux BSP (board-support package) with an integrated USB stack for the MCF5253. The 66- and 80-MHz MCF5221x cost $4.39 (10,000), and the MCF5253 costs $8.64 (10,000). The M52211EVB evaluation board costs $299, and the M5253EVBE evaluation board costs $680.

Freescale Semiconductor, www.freescale.com

EMBEDDED SYSTEMS

DVI controller targets TFT LCDs

The 5.5-mm, ultraslim DV-Slim DVI (digital-visual-interface) translator board connects TFT (thin-film-transistor) LCDs to standard-video interfaces. The device automatically converts DVI signals into TTL or LVDS (low-voltage-differential-signaling) signals for TFT LCDs and works with LCDs measuring 5 to 46 in. diagonally with 6- and 8-bit color depth; it also supports LCDs with single-channel LVDS. The DV-Slim translator board costs $49.74 (10,000).

Apollo Display Technologies, www.apollodisplays.com

Wireless embedded-networking module has remote capabilities

The MatchPort b/g secure, embedded-wireless 802.11 b/g networking-device server module enables 802.11 b/g wireless connectivity and Web services on devices with a serial interface on their host microcontroller. The networking device features a dual-processor design; one processor converts wired serial data into TCP/IP packets providing Web-server capabilities, and the other processor is an 802.11 b/g baseband and radio chip set. A built-in Web server allows remote device configuration and monitoring and provides the ability to scan and report wireless-network parameters. The MatchPort b/g costs $60 (10,000).

Lantronix, www.lantronix.com

GPS receiver suits mobile and in-vehicle-testing applications

The DAN-GPS (global-positioning-system)-receiver system adds GPS technology to the vendor's PowerDNA, UEILogger, and UEIPCA data-acquisition and -control Cubes. Suiting mobile and in-vehicle-testing applications, the device provides location, velocity, and UTC (universal-time-coordinated) real time. The GPS for the UEI Cube family costs $495.

United Electronics Industries, www.ueidaq.com

Dual three-phase bridge comes in high- and low-voltage models

Targeting brushless three-phase motors, the 7I39 dual three-phase, 250W bridge driver comes in low- and high-voltage models. The low-voltage model has a 10A rating at 25V dc per axis; the high-voltage model has a 5A rating at 50V dc per axis. Additional features include an overvoltage clamp, 0.75-times selectable overcurrent limits, and 1.5-times rated current. The 7I39H and 7I39V cost $98 (100).

Mesa Electronics, www.mesanet.com

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scope

CHART YOUR COURSE

LOOKING AHEAD

TO THE ELECTRONIC MATERIALS CONFERENCE

Think nanotubes are just carbon? Time was, materials for electronics were pretty well settled. But today, with plastics and other organic materials, increasing pressure from environmental concerns, the emergence of nanotechnology, and the growing demands IC scaling makes upon materials science, to see the future you need to look at materials, not just circuits. The best place to do that may be the Electronic Materials Conference, June 20 to 22 at Notre Dame University (www.tms.org/Meetings/Specialty/EMC07/home.html). After a plenary session in which Professor Alan Heeger from the University of California—Santa Barbara will discuss the reality of plastic solar cells, technical tracks will cover such topics as chemical and biosensors; III-Nitride devices; silicon-carbide structures; growing nanostructures; silicon, germanium, and compound nanowires; and organic transistors.

LOOKING BACK

AT AN EARLY USE OF BIOPOTENTIAL SENSORS

Developers at the recent Institute of Radio Engineers convention demonstrated an electronic iron-lung control system which enables a polio patient to use still-intact respiratory muscles. The system uses minute muscle-produced voltages produced by muscle contraction. Electrodes on the skin pick up the tiny voltages and direct them to an amplifier, which controls inlet and outlet air flow through the iron lung. As a result, the patient controls his own breathing, in contrast to the conventional system where breathing is governed by the rhythm of a motor-driven air pump. The equipment is now only experimental, but developers expect it will be produced in the near future.
—*Electrical Design News*, May 1957

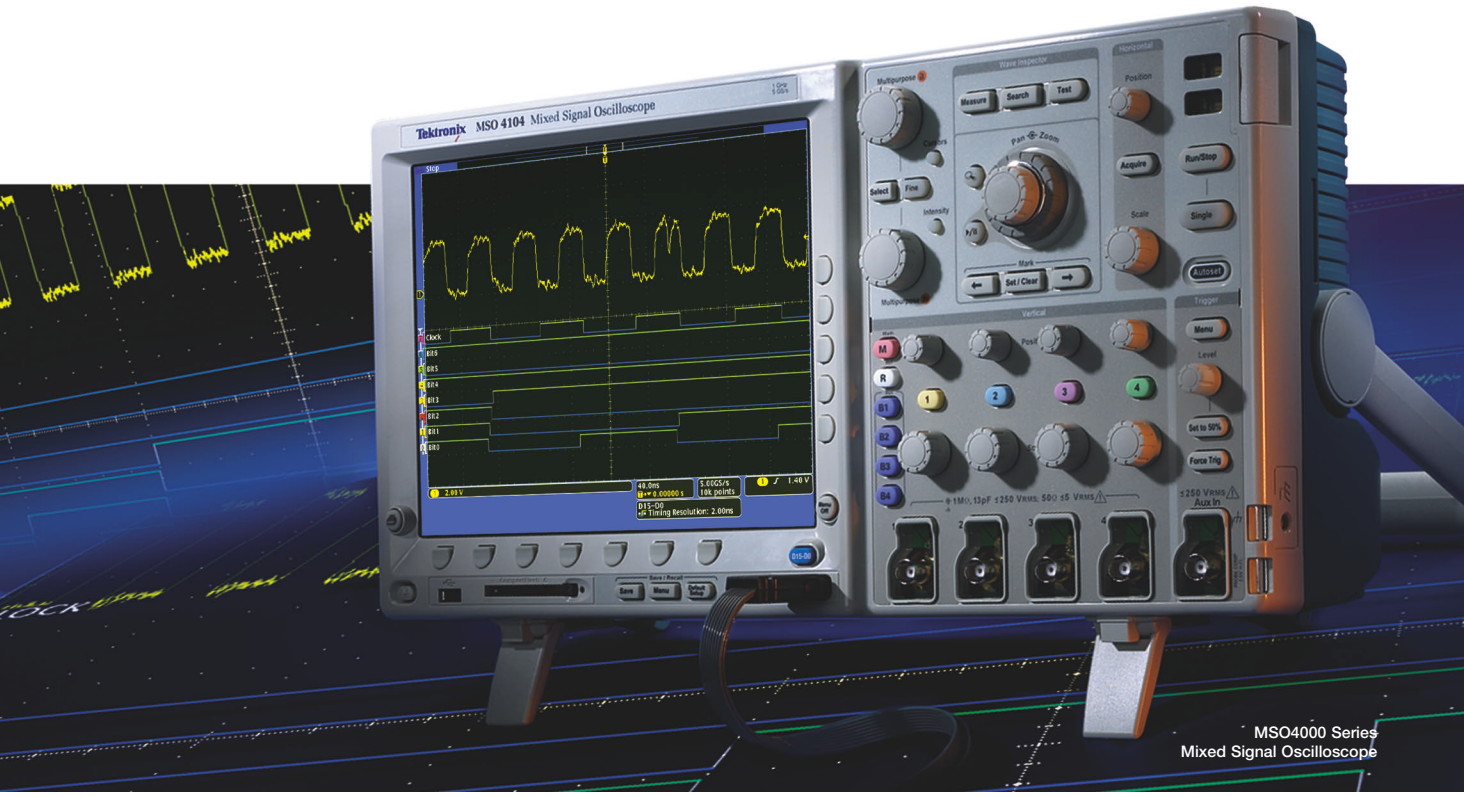
LOOKING AROUND

AT A CONSUMER-DRIVEN ELECTRONICS INDUSTRY

So consumer electronics, with its huge demands on cost and efficiency, its enormous volumes, and its fickle demand, is driving the semiconductor business. That scenario may mean the best possible news for the crafty opportunist designer. The very facts that make life so hard for a consumer-electronics company mean that very advanced technology—IBM cell processors, massive GPUs (graphics-processing units), tiny high-resolution displays, and digital cameras on chips—becomes possible, cheap, and, when demand disappears, available. Sometimes the best approach to an embedded-design problem may be massive overkill in the form of an affordable chip from an entirely different context—a cell processor as an embedded controller, a GPU as a DSP, a whole digital camera in a motion-control loop. It pays to stay informed on what's happening with all those advanced consumer ICs.

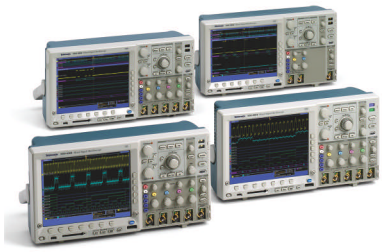
Mixed signals, one instrument.

A powerful oscilloscope with logic analyzer functionality.



Now you can visualize and correlate both analog and digital signals on one Tektronix instrument. And it's as easy to set-up and use as an oscilloscope. Meet the MSO4000 Series Mixed Signal Oscilloscope; it's a full-featured oscilloscope with basic logic analyzer functionality. Its context-rich waveform display, with either 2 or 4 analog plus 16 digital channels, enables you to simultaneously view what is going on in many points of your design. With its familiar oscilloscope operation, you will be debugging faster and easier than ever before. Relieve the pain of set-up and use. Spend more time on the task at hand. Debug faster.

Performance Specifications	
Models	MSO4032, MSO4034, MSO4054, MSO4104
Bandwidth	350 MHz, 500 MHz, 1 GHz
Channels	2 or 4 analog + 16 digital
Sample Rate on Analog Channels	Up to 5 GS/s
Max. Digital Timing Resolution	60.6 ps
Record Length	10 M points on all analog and digital channels
Display	Large 10.4 in. (264 mm) XGA screen



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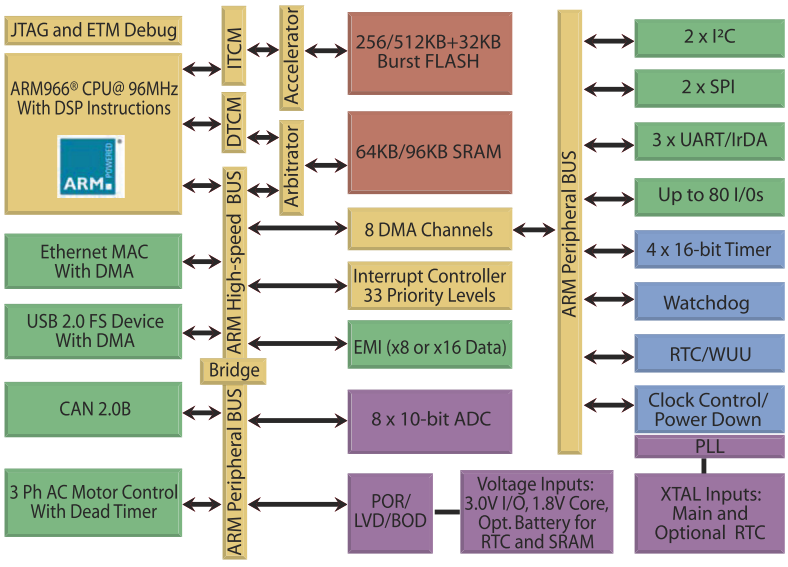

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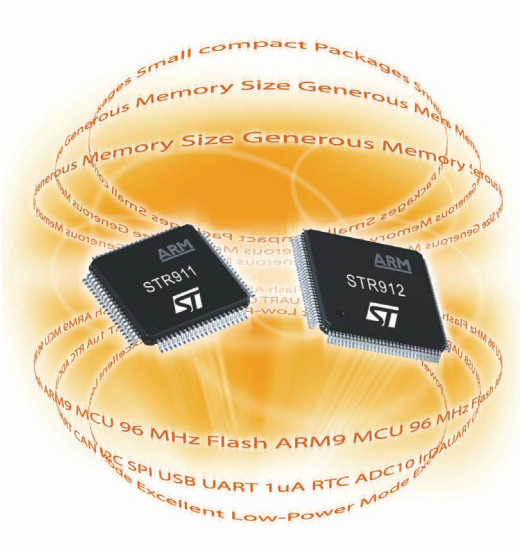

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Part Number	Flash Memory (KB)	RAM (KB)	A/D Inputs	Timer Functions		Serial Interface	GPIO (HI Current)	Package	Supply Voltage	Special Features
				(IC/OC/ PWM)	Other					
STR910FM32X	256 + 32	64	8x10-bit	7x16-bit (8,8,7)	RTC WDG	2xSPI 2xI²C 3xUART w/IrDA	40 (16)	LQFP80	Core: 1.8V I/O: 2.7 to 3.6V	CAN
STR910FW32X	256 + 32	64	8x10-bit				80 (16)	LQFP128		CAN, EMI
STR911FM42X	256 + 32	96	8x10-bit				40 (16)	LQFP80		USB, CAN
STR911FM44X	512 + 32	96	8x10-bit				40 (16)	LQFP80		USB, CAN
STR912FW42X	256 + 32	96	8x10-bit				80 (16)	LQFP128		Ethernet, USB, CAN, EMI
STR912FW44X	512 + 32	96	8x10-bit				80 (16)	LQFP128		Ethernet, USB, CAN, EMI

For further information, datasheets, and application notes, visit **www.st.com/str9**

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